Yiran Chen

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RESEARCH INTEREST

Nano-electronic devices (silicon and non-silicon)
Emerging memory and storage technologies
Embedded systems and mobile applications
Low power circuit and system
Neuromorphic computing and security

EDUCATION

Ph.D. in Electrical and Computer Engineering, Purdue University, July 2005;
Advisor: Kaushik Roy (co-chair) and Cheng-Kok Koh (co-chair)

M.S. in Electronic Engineering, Tsinghua University, January 2001 (with honor); Advisor: Chong-Cheng Fan

B.S.* in Electronic Engineering, Tsinghua University, June 1998 (with honor); Advisor: Chong-Cheng Fan

* Graduated within 4 years under a 5-year undergraduate program

PROFESSIONAL EXPERIENCE

Associate Professor, Electrical and Computer Engineering Dept., U. of Pittsburgh, Sep. 2014 – Present.
Assistant Professor, Electrical and Computer Engineering Dept., U. of Pittsburgh, Sep. 2010 – Aug. 2014.
Graduate Faculty, Electrical and Computer Engineering Dept., Purdue University, Sep. 2007 – Aug. 2012.
Staff Engineer, Memory Product Group, Seagate Technology LLC, Apr. 2007 – Aug. 2010.
Senior R&D Engineer I, PrimeTime Group, Synopsys Inc., Jul. 2005 – Apr. 2007.
Intern Engineer, Transmitter/Receiver Design Group, Micron Tech., Jun. 2003 – Aug. 2003.
Intern Engineer, Advanced System Research Group, Micron Tech., May 2002 – Aug. 2002.

GRANTS (TOTAL PERSAONAL CASH ALLOCATION: EXTERNAL-$2,632,011, INTERNAL-$47,000)

Federal Research Funding (Total personal allocation: $2,194,021)

1. ***National Science Foundation***: Yiran Chen (PI, 100%), "CSR: Small: OREO: Tri-layer Optimization for Power Efficient OLED Display," CNS-1422057, 09/01/2014-08/31/2017, $249,997.
2. ***National Science Foundation***: Qinru Qiu (Lead-PI, Syracuse, 38%), Hai Li (PI, Pitt, 31%), Yiran Chen (co-PI, Pitt, 31%), "XPS: DSD: Collaborative Research: NeoNexus: The Next-generation Information Processing System across Digital and Neuromorphic Computing Domains," XPS-1337198, 09/01/2013-08/31/2017, $725,884.
3. ***National Science Foundation***: Yiran Chen (PI, 100%), "CAREER: Centaur: A Bio-inspired Ultra Low-Power Hybrid Embedded Computing Engine Beyond One TeraFlops/Watt," CNS-1253424, 06/01/2013-05/31/2018, $450,000.
4. ***National Science Foundation***: Yiran Chen (lead-PI, 50%), Yuan Xie (PI, PSU, 50%), "SHF: Small: Collaborative Research: STEMS: STatistic Emerging Memory Simulator," CCF-1217947, 07/01/2012-06/30/2015, $300,000.
5. ***National Science Foundation***: Hai Li (lead-PI, NYU-Poly, 50%), Yiran Chen (PI, 50%), "Collaborative Research: SMURFS: Statistical Modeling, SimUlation and Robust Design Techniques For MemriStors," ECCS-1202225, 05/01/2012-04/30/2015, $500,149.

6. ***National Science Foundation***: Hai Li (lead-PI, NYU-Poly, 50%), Yiran Chen (PI, 50%), "CSR: Small: Collaborative Research: Cross-Layer Design Techniques for Robustness of the Next-Generation Nonvolatile Memories," CNS-1116171, 09/01/2011-08/31/2015 (extended by 12 months), $450,000.
7. ***Air Force Research Lab***: Yiran Chen (PI, 50%), Hai Li (co-PI, 50%), "The Design of Neuromorphic Controller System Built with Memristor Crossbars," TBD, TBD, $300,000.
8. ***Air Force Research Lab***: Hai Li (PI, 50%), Yiran Chen (co-PI, 50%), "The Design of Neuromorphic Controller System Built with Memristor Crossbars," FA8750-15-2-0048, 01/01/2015-12/31/2017, $750,000.
9. ***Air Force Research Lab***: Hai Li (PI, 50%), Yiran Chen (co-PI, 50%), "Neuromorphic Computing Engine with Resistive Crossbar Architecture," FA8750-14-1-0241, 09/19/2014-02/19/2015, $118,047.
10. ***Air Force Research Lab***: Yiran Chen (PI, 50%), Hai Li (co-PI, 50%), "Memristor Crossbar Based Computing Engine for High Performance and Power Efficiency," FA8750-13-2-0115, 08/01/2013-10/31/2013, $50,000.
11. ***Air Force Research Lab***: Yiran Chen (PI, 100%), "Design for Manufacturing Method for Memristor-based Neuromorphic Computing Processors," FA8750-11-1-0271, 10/01/2011-09/30/2012, $35,000.

Awards and Scholarships(Total personal allocation: $24,000)

12. ***49th Design Automation Conference A. Richard Newton Scholarship***: Yiran Chen (PI, 100%), "NVSim-VX: Variation Aware Emerging Nonvolatile Memory Simulator," $24,000, 06/01/2012-05/31/2014. Student recipient: **Wujie Wen**. (Peer reviewed)

Industry Funding (Total personal allocation: $360,000)

13. ***Samsung Global MRAM Innovation*****:** Yiran Chen (PI, 100%), "ECC Designs for High-Performance High-Reliable STT-MRAM," $90,000, 02/01/2014-01/31/2015. (Peer reviewed).
14. ***HP Lab Innovation Research Program*****:** Yiran Chen (PI, 100%), "Memristor Crossbar Based Neuromorphic Hardware Systems," $250,000, 10/01/2012-09/30/2015. (Peer reviewed).
15. ***Qualcomm*****:** Hai Li (PI, 50%), Yiran Chen (co-PI, 50%), $40,000. (Gift)

Small Business Innovation Research (Total personal allocation: $50,000)

16. ***National Science Foundation SBIR*****:** Yiran Chen (PI of subaward), "Novel Capacitor-less DRAM Technology with Energy Efficiency, Manufacturability, and Scalability," IIP-1448305, subawarded from Alacrity Semiconductor, $50,000, 01/01/2015-06/30/2015.

Internal Funding – University of Pittsburgh (Total personal allocation: $47,000)

17. ***Innovation Works TCC University Grant:*** Yiran Chen (PI, 100%), "Invisible Shield: Device Security via Gesture Authentication," $25,000, 09/01/2014-06/30/2015.
18. ***Pitt Ventures – 1st Gear 1st Gear Enterprise Creation Team (EC Team) Program:*** Yiran Chen (PI, 100%), "The Invisible Shield: User Classification and Authentication for Mobile Device Based on Continuous Gesture Recognition," $6,000, 01/01/2014-06/30/2014.
19. ***Central Research Development Fund***: Yiran Chen (PI, 100%), "Sub-10ns STT-RAM Switching: A Statistical Memory Cell Design View," $16,000, 07/01/2011-06/30/2013. (Peer reviewed)

Federal Research Development Grants

20. ***National Science Foundation***: Alex Jones (PI), Yiran Chen (co-PI), Steve Levitan (co-PI), Jun Yang (co-PI), "Planning Grant: I/UCRC for Nexys: Next Generation Electronic System Design," IIP-1161008, 04/15/2012-03/31/2013, $11,500.

Education Grants (Total personal allocation $4000 plus $2000 equipment)

21. ***Cornell Cup USA 2013***: James Lyle (Primary Advisor), and Yiran Chen (Advisor), "Koalakollar: Squad Tracking and Isolation Event Alert System," Student Team Members: Kent W. Nixon, Xiang Chen, Fan Mi, Ping Lang, and Natalie Janosik, $1500 cash plus $1000 equipment (two FPGA boards with $500 value each).
22. ***Cornell Cup USA 2012***: Yiran Chen (Primary Advisor), Mingui Sung (Advisor), and Ervin Sejdic (Advisor), "PandaCare: A Wearable Electronic Unit for Dementia Care," Student Team Members: Chengliu Li, Yicheng Bai, Ping Lang, Meng Li, $2500 cash plus $1000 equipment (two FPGA board with $500 value each).

International Collaborations (note: the program policy restricts the funding usage outside the country)

23. ***National Program on Key Basic Research Project (973 Program)***: Yiran Chen (Senior Personnel, 0%, PI: Hanming Wu), "Physical Study and Development on Nano-magnetic Spintronic Memory and Semiconductor Silicon-based Quantum Dot Memory," 2010CB934400, China, $3.14M, 01/01/2010-08/31/2014.

AWARDS AND HONORS

SINCE SEP. 2010

1. **Fellow of Air Force Office of Sponsored Research (AFOSR) Summer Faculty Fellowship Program (SFFP)**, AFRL/RIB, Rome, NY, 2015.
2. **Best Paper Nomination**, Design Automation Conference (DAC) for the paper entitled "An EDA Framework for Large Scale Hybrid Neuromorphic Computing Systems", 2015.
3. ***Outstanding New Faculty Award* of ACM's Special Interest Group on Design Automation (SIGDA)**, 2014.
4. **Best Paper Nomination**, Design Automation Conference (DAC) for the paper entitled "State-Restrict MLC STT-RAM Designs for High-Reliable High-Performance Memory System", 2014.
5. Invitee of **2013 U.S. Frontiers of Engineering Symposium (FOE) of National Academy of Engineering (NAE)**.
6. ***NSF CAREER Award*, 2013.**
7. **49th Design Automation Conference A. Richard Newton Scholarship** for Ph.D. student Wujie Wen, 2012.
8. **Three Times Air Force Visiting Faculty Research Program (VFRP) Fellowship**, AFRL/RIB, Rome, NY, 2011, 2012, 2013. (Selected extended grants of total $37K are also approved for 2011-2013).
9. **Best Paper Award,** Great Lakes Symposium on VLSI (GLSVLSI) for the paper entitled "Coordinating Prefetching and STT-RAM based Last-level Cache Management for Multicore Systems", 2013.
10. **Best Paper Nomination**, Asia and South Pacific Design Automation Conference (ASP-DAC) for the paper entitled "Prefetching Techniques for STT-RAM based Last-level Cache in CMP Systems", 2014.
11. **Best Paper Nomination**, Asia and South Pacific Design Automation Conference (ASP-DAC) for the paper entitled "Compiler-Assisted Refresh Minimization for Volatile STT-RAM Cache", 2013.
12. **Best Paper Nomination**, Asia and South Pacific Design Automation Conference (ASP-DAC) for the paper entitled "Geometry Variations Analysis of TiO_2 Thin Film and Spintronic Memristors", 2011.

BEFORE SEP. 2010

13. ***Best Paper Award***, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED) for the paper entitled "Combined Magnetic- and Circuit-level Enhancements for the Nondestructive Self-Reference Scheme of STT-RAM", 2010.
14. **Best Paper Nomination,** Design, Automation & Test in Europe Conference and Exhibition (DATE) for the paper entitled "A Nondestructive Self-Reference Scheme for Spin-Transfer Torque Random Access Memory (STT-RAM)", 2010.
15. **Best Paper Nomination,** the 11th International Symposium on Quality Electronic Design (ISQED) for the paper entitled "Scalability of PCMO-based Resistive Switch Device in DSM Technologies", 2010.
16. ***Best Paper Award***, the 9th International Symposium on Quality Electronic Design (ISQED) for paper entitled "Design Margin Exploration of Spin-Torque Transfer RAM (SPRAM)", 2008.
17. **Best Paper Nomination,** the 6th International Symposium on Quality Electronic Design (ISQED) for the paper entitled "Power Supply Noise-aware Scheduling and Allocation for DSP Synthesis", 2005.
18. **Finalists of Prestigious 2007 DesignVision Awards** for PrimeTimeVX, International Engineering Consortium, 2007.
19. **The hot 100 products of 2006** for PrimeTimeVX, EDN (www.edn.com), 2006.
20. **PrimeTimeVX - EDN 100 Hot Products Distinction**, Synopsys Inc., 2006.

PLENARY TALKS

1. The 20th National Conference of Information Storage (NCIS), Beijing, 2014.

PROFESSIONAL SERVICE ACTIVITIES

University Committee

1. Chair, ECE Technical Area Committee (Computers), 2014-
2. ECE Graduate Curriculum and Program Committee, 2012-2015
3. ECE Technical Area Committee (Computers), 2012-2014
4. Faculty Search Committee, 2011, 2012, 2015

5. ECE Undergraduate lab Committee, 2011-2012
6. ECE Undergraduate Committee, 2011-2012

Journal Editor

1. Associate Editor, IEEE Transactions on CAD of Integrated Circuits and Systems (TCAD), 2012.01-.
2. Associate Editor, ACM Journal on Emerging Technologies in Computing Systems (JETC), 2012.01-.
3. Associate Editor, ACM SIGDA e-News, 2013.06-
4. Editor, Journal of Convergence Information Technology (JCIT), 2008-.

Conference General Chair and Steering Committee (Including Workshops)

1. IEEE Non-Volatile Memory Systems and Applications Symposium (NVMSA), 2014-. (Steering Committee Member)
2. 2015 Frontier of Information Storage and Design Automation Technologies Workshop, May 2015. (Co-chair)
3. Cloud·Storage·Big Data Summit, Jul. 2013. (General Chair)
4. Asian Nonvolatile Memory Workshop (ANVMW), Jul. 2013. (General Chair)
5. Asian Nonvolatile Memory Workshop (ANVMW), Jul. 2012. (Vice General Chair)
6. 5th International Workshop on Emerging Circuits and Systems (IWECS), 2013. (Vice Chair)

Conference/Session/Tutorial Organizer

1. ACM SIGDA Outstanding New Faculty Award (ONFA) selection committee, 2015.
2. Chair, Student Research Forum of Asia and South Pacific Design Automation Conference (ASP-DAC), 2015.
3. Design contest chair/co-chair, International Symposium on Low Power Electronics and Design (ISLPED), 2011-2014.
4. Special session chair, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2016.
5. Publicity chair, IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA), 2014.
6. Best paper selection committee, IEEE Transactions on CAD of Integrated Circuits and Systems (TCAD), 2015.
7. Best paper selection committee, International Conference on Computer-Aided Design (ICCAD), 2014.
8. Best paper selection committee, International Conference on VLSI Design (VLSI Design), 2013.
9. Tutorial organizer, 25th International System-on-Chip Conference: Neuromorphic Computing: A SoC Scaling Path for the Next Decade, 2012
10. Tutorial organizer, the 21st International Conference on Parallel Architectures and Compilation Techniques (PACT), 2012: Emerging Nonvolatile Memory Applications in Computer Architecture. (Cancelled)
11. Special session organizer, Great Lakes Symposium on VLSI (GLSVLSI), 2015: Neuromorphic Computing based on Resistive Devices.
12. Special session co-organizer, Design Automation Conference (DAC), 2014: Wearable Technology for Health and Well-Being: From Ultra-Low Power Integrated Sensors to Enterprise Applications.
13. Special session organizer, International Conference on Computer-Aided Design (ICCAD), 2013: Emerging Design Automation (EDA): The Movement to Apply CAD Techniques to Global Challenges.
14. Special session organizer, Asia and South Pacific Design Automation Conference (ASP-DAC), 2013: Emerging Security Topics in Electronic Designs and Mobile Devices.
15. Special session co-organizer, Design Automation Conference (DAC), 2012: Brain-inspired Autonomous Computing and Modeling.
16. Special session organizer, International Conference on Computer-Aided Design (ICCAD), 2011: Emerging Nonvolatile Memory and Memristors.
17. Hot session organizer, Design, Automation & Test in Europe Conference and Exhibition (DATE), 2010: Memristor: Device, Design and Application.

Technical Program Chair, Track Chair/Co-chair

1. TPC Chair, 6th Asia Symposium on Quality Electronic Design (ASQED 2015), 2015.
2. TPC Track Chair, Memory: Technology Circuit, and System, VLSI-SoC, 2015.
3. TPC Track Chair, Cognitive Computing in Hardware (CCH), International Symposium on Quality Electronic Design (ISQED), 2015.
4. TPC Track Chair, Emerging Process & Device Technologies and Design Issues (EDT), International Symposium on Quality Electronic Design (ISQED), 2015.
5. TPC Track Chair, Emerging Technologies, Asia and South Pacific Design Automation Conference (ASP-DAC), 2015-2016.
6. TPC Track Chair, Data Storage Technology and Applications (DSTA) Symposium, International Conference on Computing, Networking and Communications (ICNC), 2014.
7. TPC Track Chair, Emerging Technologies, International Conference on VLSI Design (VLSI Design), 2013, 2016.
8. TPC Track Chair, Architecture Track, IEEE International Conference on Networking, Architecture, and Storage (NAS), 2012.
9. TPC Track Chair, Bio Electronics Track, Asia Symposium and Exhibits on Quality Electronic Design (ASQED), 2010-2011.

Technical Program Committee Member

1. ACM Student Research Competition (SRC) at ICCAD, 2013-2014.
2. Adaptive Learning On-a-chip: Hardware and Algorithms, (ALOHA), 2015.
3. Asia and South Pacific Design Automation Conference (ASP-DAC), 2011-2013, 2015.
4. Asia Symposium and Exhibits on Quality Electronic Design (ASQED), 2010-2013.
5. CSI International Symposium on Computer Architecture & Digital Systems (CADS), 2015.
6. Design Automation Conference (DAC), 2012-2014.
7. Design, Automation & Test in Europe (DATE), 2010-2014.
8. IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2009-2010, 2012.
9. IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), 2013-2014.
10. IEEE International Conference on Embedded Software and Systems (ICESS), 2011.
11. IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA), 2013-2015.
12. IEEE International Conference on Networking, Architecture, and Storage (NAS), 2012.
13. IEEE International Symposium on Circuits and Systems (ISCAS), 2008-2010.
14. IEEE Symposium on Computational Intelligence for Security and Defense Applications (CISDA), 2015.
15. IEEE Symposium on Embedded Systems for Real-Time Multimedia (ESTIMedia), 2011-2015.
16. IEEE Workshop on GREEN Multimedia: Energy-efficient Multimedia Computing, Communication and Presentation, 2013.
17. IEEE Workshop on Signal Processing Systems, 2014.
18. International Conference on ASIC (ASICON), 2015.
19. International Conference on Communications, Circuits and Systems (ICCCS), 2010.
20. International Conference on Computing, Networking and Communications (ICNC), 2014.
21. International Conference on Field Programmable Logic and Applications (FPL), 2008-2011.
22. International Conference on Field-Programmable Technology (FPT), 2007-2014.
23. International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), 2012-2015.
24. International Conference on Neural Information Processing (ICONIP), 2012.
25. International Conference on VLSI Design (VLSI Design), 2010-2015.
26. International Electronic Design Education Conference (IEDEC), 2012-2014.
27. International Symposium on Low Power Electronics and Design (ISLPED), 2007-2015.
28. International Symposium on Quality Electronic Design (ISQED), 2008-2014.
29. International Symposium on Quality Electronic Design in China (ISQED-China), 2014

30. International Symposium on VLSI Design, Automation and Test (VLSI-DAT), 2015.
31. International Workshop on Neuromorphic and Brain-Based Computing Systems (NeuComp), 2013, 2015.
32. International Workshop on Non-Volatile Memory (INVM), 2013.
33. International Workshop on Smart Embedded Systems (SES), 2014
34. Memory Architecture and Organization Workshop (MeAOW), 2011-2013.
35. The 15th Non-Volatile Memory Technology Symposium (NVMTS), 2015.
36. Workshop on Emerging Supercomputing Technologies (WEST, in conjunction with International Conference on Supercomputing), 2011.
37. Workshop on Hardware and Architectural Support for Security and Privacy (HASP), 2014.

Conference Session Chair

1. Discussion Leader, the Spin Dynamics in Nanostructures Gordon Research Conferences (GRC), 2015.
2. Great Lakes Symposium on VLSI (GLSVLSI), 2015.
3. Asia and South Pacific Design Automation Conference (ASP-DAC), 2012-2014.
4. Asia Symposium and Exhibits on Quality Electronic Design (ASQED), 2010.
5. Design Automation Conference (DAC), 2012, 2014.
6. Design, Automation & Test in Europe (DATE), 2010-2013.
7. IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2011, 2013.
8. International Conference on Compilers, Architecture and Synthesis for Embedded Systems (CASES), 2013.
9. International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), 2013.
10. International Conference on Neural Information Processing (ICONIP), 2012.
11. International Symposium on Low Power Electronics and Design (ISLPED), 2007, 2011, 2013-2014.
12. International Symposium on Quality Electronic Design (ISQED), 2007-2008.

Journal and Conference Referee

1. PLOS ONE
2. ACM Transactions on Design Automation of Electronic Systems (TODAES)
3. ACM Transactions on Embedded Computing Systems (TECS)
4. ACM Journal of Emerging Technologies in Computing (JETC)
5. Cognitive Computation
6. Design Automation for Embedded Systems
7. EURASIP Journal on Advances in Signal Processing (EURASIP)
8. IEEE Electron Device Letters (EDL)
9. IEEE Embedded System Letters (ESL)
10. IEEE Design & Test of Computers (D&T)
11. IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)
12. IEEE Journal of Solid State Circuits (JSSC)
13. IEEE Sensors Journal (Sensors)
14. IEEE Transactions on Automatic Control (TACON)
15. IEEE Transactions on CAD of Integrated Circuits and Systems (TCAD)
16. IEEE Transactions on Circuit and Systems I (TCAS-I)
17. IEEE Transactions on Circuit and Systems II (TCAS-II)
18. IEEE Transactions on Computers (TC)
19. IEEE Transactions on Electron Devices (TED)
20. IEEE Transactions on Nanotechnology (TNANO)
21. IEEE Transactions on Neural Networks and Learning Systems (TNNLS)
22. IEEE Transactions on Parallel and Distributed Systems (TPDS)
23. IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)
24. IET Circuits, Devices & Systems (IET-CDS)

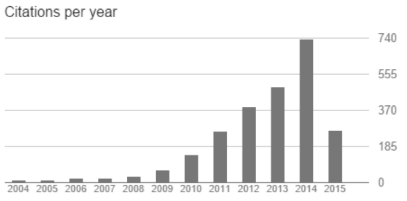
25. IET Computers & Digital Techniques (IET-CDT)
26. Iranian Journal of Fuzzy Systems (IJFS)
27. Journal of Circuits, Systems, and Computers (JCSC)
28. Journal of Computer Science and Technology (JCST)
29. Journal of Low Power Electronics (JOLPE)
30. Journal of Medical and Biological Engineering (JMBE)
31. Materials Science in Semiconductor Processing (MSSP)
32. Microelectronics Journal (MEJ)
33. Microprocessors and Microsystems (MICPRO)
34. Nature Communications
35. Naturwissenschaften (NAWI)
36. Neural Computing and Applications (NCAA)
37. Neural Networks
38. The VLSI Journal on Integration
39. Science China
40. Asia and South Pacific Design Automation Conference (ASP-DAC)
41. Design, Automation & Test in Europe Conference and Exhibition (DATE)
42. IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)
43. IEEE International Magnetics Conference (Intermag)
44. IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)
45. IEEE International Symposium on Circuits and Systems (ISCAS)
46. IEEE Real-Time Systems Symposium (RTSS)
47. IEEE Symposium Series on Computational Intelligence (SSCI)
48. International Conference on VLSI Design (VLSI Design)
49. International Conference on Microelectronics (IEEE ICM)
50. International Joint Conference on Neural Networks (IJCNN)
51. International Symposium on High-Performance Computer Architecture (HPCA)

Other Services

1. Panelist for Department of Energy (DOE).
2. Ad Hoc Reviewer of National Science Foundation (NSF) Experimental Program to Simulate Competitive Research (EPSCoR) Proposal.
3. Ad Hoc Reviewer of Research Grants Council (RGC) of Hong Kong Proposal.
4. Ad Hoc Reviewer of Partner University Fund (French-American projects).
5. Reviewer of University of Missouri Research Board proposal/award.
6. External reviewer of Public Sector Funding Research Scheme (PSF) of Science & Engineering Research Council (SERC), the Agency for Science, Technology & Research (A*STAR), Singapore.
7. Patent Review Board Member, Memory Product Group, Seagate Technology, 2007–2010.

LIST OF PUBLICATIONS

I. Google Citations (It may deviate from other records): 2455



Note: * and # in front of the author's names indicates the student supervised and co-supervised by me, respectively. If neither my students nor I are the first author of the publications, usually that is the collaborative work led by some other researchers. + indicates the visiting scholar whose work is mainly done during the visit to my lab.

II. Books (Total: 1)

B1. H. Li, and Y. Chen, *Nonvolatile Memory Design: Magnetic, Resistive, and Phase Changing*, CRC Press, Dec. 19, 2011. ISBN: 978-14-398-0745-3.

III. Book Chapters (Total: 11)

SINCE SEP. 2010

Ch1. Y.-C. Chen, W. Zhang, Y. Chen, and H. Li, *In-place Logic Obfuscation for Emerging Nonvolatile FPGAs*, (in Fundamentals of IP and SoC Security –Design, Verification, and Debug), Springer, to appear.

Ch2. *K. Nixon, L. Chen, Y. Chen, and Z.-H. Mao, *User Classification and Authentication for Mobile Device Based on Continuous Gesture*, (in Security of Mobile Cloud Computing, Editor: Dr. Keesook Han), Springer, to appear.

Ch3. *W. Wen, *Y. Zhang, and Y. Chen, *Statistical Reliability/Energy Characterization in STT-RAM Cell Designs*, (in Spintronics Based Computing, Editor: Weisheng Zhao and Guillaume Prenat), Springer, Jun. 14, 2015. ISBN: 978-3-319-15179-3.

Ch4. *P. Wang, E. Eken, W. Zhang, R. Joshi, R. Kanj, and Y. Chen, *A Thermal and Process Variation Aware MTJ Switching Model and Its Applications in Soft Error Analysis*, (in More than Moore Technologies for Next Generation Computer Design, Editor: Rasit O. Topaloglu), Springer, Feb. 20, 2015. ISBN: 978-14-939-2162-1.

Ch5. *Y. Zhang, W. Wen, H. Li, and Y. Chen, *The Prospect of STT-RAM Scaling*, (in Metallic Spintronic Devices, Editor: Xiaobin Wang), CRC Press, Aug. 4, 2014. ISBN: 978-14-665-8844-8.

Ch6. Y. Chen, H. Li and Z. Sun, *Spintronic Memristor as Interface between DNA and Solid State Devices*, (in Memristors and Memristive Systems, Editor: Ronald Tetzlaff), Springer, Jan. 1, 2014. ISBN: 978-1-4614-9067-8.

Ch7. Y. Chen, *J. Guo, and Z. Sun, *CPU-GPU System Designs for High Performance Computing*, (in High Performance Semantic Cloud Auditing, Editor: Keesook Han and Baek-Young Choi), Springer, Aug. 31, 2013. ISBN: 978-14-614-3295-1.

Ch8. *Y. Zhang, *W. Wen, and Y. Chen, *Asymmetry in STT-RAM Cell Operations*, (in Emerging Memory Technologies: Design, Architecture, and Applications, Editor: Yuan Xie), Springer, Aug. 31, 2013. ISBN: 978-14-419-9550-6.

Ch9. *K. Nixon, Y. Chen, Z.-H. Mao, and K. Li, *User Classification and Authentication for MOBILE Device Based on Gesture Recognition*, (in "Network Science and Cybersecurity", Editor: Robinson Pino), Springer, Jun. 27, 2013. ISBN: 978-14-6147-596-5.

Ch10. Y. Chen, H. Li, Y. Xie, and D. Niu, *Low Power Design of Emerging Memory Technologies*, (in Handbook of Energy-Aware and Green Computing, edited by Ishfaq Ahmad and Sanjay Ranka), CRC Press, Jan. 24, 2012. ISBN: 978-14-398-5040-4.

BEFORE SEP. 2010

Ch11. X. Wang, Y. Chen and T. Zhang, *Magnetization Switching in Spin Torque Random Access Memory: Challenges and Opportunities*, (in "CMOS Processors and Memories", Editor: Iniewski, Krzysztof), Springer, Aug. 22, 2010. ISBN: 978-90-481-9215-1.

IV. Invited Journal Articles (Total: 3)

SINCE SEP. 2010

IJ1. L. Zhang, N. Ge, J. J. Yang, Z. Li, R.S. Williams, and Y. Chen, "Low Voltage Two-state-variable Memristor Model of Vacancy-drift Resistive Switches," *Applied Physics A: Materials Science & Processing (APA)*, vol. 119, no. 1, Apr. 2015, pp.1-9. DOI: 10.1007/s00339-015-9033-3。

IJ2. Y. Chen, H. Li, C. Wu, *B. Liu, C. Liu, #M. Mao, and *W. Wen, "Neuromorphic Computing based on Emerging Devices," *Communication of China Computer Federation (CCCF)*, to appear. (in Chinese)

IJ3. Y. Chen, W. Zhao, Z. Sun, and *Y. Zhang, "Emerging Nonvolatile Memory," *Modern Physics*, to appear. (in Chinese)

V. Refereed Journal Articles (Total: 47)

SINCE SEP. 2010

J1. B. Li, P. Gu, Y. Shan, Y. Wang, Y. Chen, and H. Yang, "RRAM-based Analog Approximate Computing," *IEEE Transactions on CAD of Integrated Circuits and Systems (TCAD)*, to appear.

J2. Y. Zhang, B.N. Yan, W. Kang, Y.Q. Cheng, J-O Klein, Y.G. Zhang, Y. Chen and W.S. Zhao, "Compact Model of Subvolume MTJ and its Design Application at Nanoscale Technology Nodes," *IEEE Transactions on Electron Devices*, to appear. DOI: 10.1109/TED.2015.2414721.

J3. D. Wang, H.-P. Liu, and Y. Chen, "Multi-bit Soft Error Tolerable L1 Data Cache Based on Characteristic of The Data Value," *Journal of Central South University*, to appear.

J4. Q. Li, J. Li, L. Shi, C. J. Xue, Y. Chen, and Y. He, "Compiler-Assisted Refresh Minimization for Volatile STT-RAM Cache," *IEEE Transactions on Computers (TC)*, to appear. DOI: 10.1109/TC.2014.2360527.

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VI. Journal Briefs and Extended Abstracts (Total: 5)

SINCE SEP. 2010

Ja1. *Y. Zhang, Y. Li, Z. Sun, H. Li, Y. Chen, and Alex K. Jones, "Read Performance: The Newest Barrier in Scaled STT-RAM," *IEEE Transactions on Very Large Scale Integration (TVLSI) Systems*, to appear. DOI: 10.1109/TVLSI.2014.2326797.

Ja2. M. Zhao, Y. Chen, X. Chen, and C. Xue, "Online OLED Dynamic Voltage Scaling for Video Streaming Applications on Mobile Devices," *ACM SIGBED Review*, vol. 10, no. 2, 2013, pp. 18. DOI: 10.1145/2518148.2518156.

Ja3. L. Niu, L. Medina, and Y. Chen, "Reliability-aware Energy Minimization for Real-time Embedded Systems with Window-constraints," *ACM SIGBED Review*, vol. 10, no. 2, 2013, pp. 26. DOI: 10.1145/2518148.2518164.

Ja4. Y. Chen, H. Li, C.-K. Chen, K. Roy, J. Li and G. Sun, "Variable-Latency Adder (VL-Adder): New Arithmetic Circuit Design Practice for Low Power and NBTI Tolerance," *IEEE Transactions on Very Large Scale Integration (TVLSI) Systems,* vol. 18, no. 11, Oct. 2010, pp. 1621-1624. DOI: 10.1109/TVLSI.2009.2026280.

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Ja5. Y. Chen, H. Li, C.-K. Chen and K. Roy, "Gated Decap: Gate Leakage Control of On-chip Decoupling Capacitors in Scaled Technologies," *IEEE Transactions on Very Large Scale Integration (TVLSI) Systems*, vol. 17, no. 12, Dec. 2009, pp. 1749-1752. DOI: 10.1109/TVLSI.2008.2007843.

VII. Invited Conference Publications (Total: 28)

SINCE SEP. 2010

Ci1. *B. Liu, Q. Wu, H. Li, Q. Qiu, and Y. Chen, "Cloning Your Mind: Security Concerns in Cognitive System Designs and Their Solutions," *Design Automation Conference (DAC)*, Jun. 2015, to appear.

Ci2. H. Li, B. Liu, X. Liu, M. Mao, Y. Chen, Q. Wu, and Q. Qiu, "The Applications of Memristor Devices in Next-generation Cortical Processor Designs," *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2015, to appear.

Ci3. *W. Wen, B. Li, and Y. Chen, "EDA Challenges for Memristor-Crossbar based Neuromorphic Computing," *Great Lakes Symposium on VLSI (GLVLSI)*, May 2015, to appear.

Ci4. Y. Zhang, W. Wu, Y. Chen, "Spintronic Logic Gates Based on Giant Spin Hall Effect (GSHE) MTJ Element," *Design, Automation & Test in Europe (DATE)*, Mar. 2015, pp. 1000-1005. ISBN: 978-3-9815-3704-8.

Ci5. H. Li, X. Liu, M. Mao, Y. Chen, Q. Wu, and M. Barnell, "Neuromorphic Hardware Acceleration Enabled by Emerging Technologies," *International Symposium on Integrated Circuits (ISIC)*, Dec. 2014, pp. 124-127. DOI: 10.1109/ISICIR.2014.7029530. (Peer reviewed)

Ci6. *I. Bayram and Y. Chen, "NV-TCAM: Alternative Interests and Practices in NVM Designs," *IEEE Non-Volatile Memory Systems and Applications Symposium (NVMSA)*, Aug. 2014, pp. 1-6. DOI: 10.1109/NVMSA.2014.6927206

Ci7. *W. Wen, *Y. Zhang, #M. Mao, and Y. Chen, "STT-RAM Reliability Enhancement through ECC and Access Scheme Optimization," *The 18th International Symposium on Consumer Electronics (ISCE)*, Jun. 2014, pp. 22-25. DOI: 10.1109/ISCE.2014.6884324.

Ci8. *X. Chen, Y. Chen, M. Dong, and C. Zhang, "Demystifying Energy Usage in Smartphones," *Design Automation Conference (DAC)*, Jun. 2014, pp. 1-5. DOI: 10.1145/2593069.2596676.

Ci9. M. Sun, L. E. Burke, Z.-H. Mao, Y. Chen, H.-C. Chen, Y. Bai, Y. Li, C. Liu, and W. Jia, "eButton: A Wearable Computer for Health Monitoring and Personal Assistance," *Design Automation Conference (DAC)*, Jun. 2014, pp. 1-6. DOI: 10.1145/2593069.2596678.

Ci10. Q. Wu, *B. Liu, Y. Chen, H. Li, Q. Chen, and Q. Qiu, "Bio-Inspired Computing with Resistive Memories – Models, Architectures and Applications," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Jun. 2014, pp. 834-837. DOI: 10.1109/ISCAS.2014.6865265. (Peer reviewed)

Ci11. D. Wang, J. Guo, K. Bu, and Y. Chen, "Reduction of Data Prevention Cost and Improvement of Reliability in MLC NAND Flash Storage System," *Data Storage Technology and Applications (DSTA) Symposium, International Conference on Computing at Networking and Communications (ICNC)*, Feb. 2014, pp. 259-263. DOI: 10.1109/ICCNC.2014.6785342.

Ci12. A. Jones, Y. Chen, W.O. Collinge, H. Xu, L. Schaefer, A.E. Landis, and M.M. Bilec, "Considering Fabrication in Sustainable Computing," *International Conference on Computer Aided Design (ICCAD)*, Nov. 2013, pp. 206-210. DOI: 10.1109/ICCAD.2013.6691120.

Ci13. B. Li, M. Hu, Y. Wang, Y. Chen and H. Yang, "Memristor-based Approximated Computation," *International Symposium on Low Power Electronics and Design (ISLPED)*, Sep. 2013, pp. 242-247. DOI: 10.1109/ISLPED.2013.6629302.

Ci14. *Y. Zhang, *L. Zhang, and Y. Chen, "MLC STT-RAM Design Considering Probabilistic and Asymmetric MTJ Switching," *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2013, pp. 113-116. DOI: 10.1109/ISCAS.2013.6571795. (Peer Reviewed)

Ci15. *K. Nixon, *X. Chen, Z.-H. Mao, Y. Chen, and K. Li, "Mobile User Classification and Authorization Based on Gesture Usage Recognition," *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2013, pp. 384-389. DOI: 10.1109/ASPDAC.2013.6509626.

Ci16. Y. Chen, *X. Chen, M. Zhao, and J. Xue, "Mobile Devices User - The Subscriber and also the Publisher of Real-Time OLED Display Power Management Plan," *International Conference on Computer Aided Design (ICCAD),* Nov. 2012, pp. 687-690. DOI: 10.1145/2429384.2429534.

Ci17. Z. Shao, Y. Liu, Y. Chen, and T. Li, "Utilizing PCM for Energy and Power Optimization in Embedded Systems," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Aug. 2012, pp. 398-403. DOI: 10.1109/ISVLSI.2012.81.

Ci18. R. Pino, H. Li, Y. Chen, M. Hu and *B. Liu, "Statistical Memristor Modeling and Case Study in Neuromorphic Computing," *Design Automation Conference (DAC)*, Jun. 2012, pp. 585-590. DOI: 10.1145/2228360.2228466.

Ci19. Y. Chen, *Y. Zhang and *P. Wang, "Probabilistic Design in Spintronic Memory and Logic Circuit," *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2012, 323-328. DOI: 10.1109/ASPDAC.2012.6164967.

Ci20. J. Xue, Y. Zhang, Y. Chen, G. Sun, J. J. Yang, and H. Li, "Emerging Non-Volatile Memories: Opportunities and Challenges," *International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Oct. 2011, pp.325-334. DOI: 10.1145/2039370.2039420.

Ci21. Y. Chen, and H. Li, "Emerging Sensing Techniques for Emerging Memories," *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2011, pp. 204-210. DOI: 10.1109/ASPDAC.2011. 5722185.

Ci22. Y. Chen, H. Li, X. Wang, and J. Park, "Applications of TMR Devices in Solid State Circuits and Systems," *International SoC Design Conference (ISOCC)*, Nov. 2010, S14-2. DOI: 10.1109/SOCDC.2010. 5682923.

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Ci23. Y. Chen, X. Wang, Z. Sun, H. Li, "The Application of Spintronic Devices in Magnetic Bio-sensing," *Asia Symposium on Quality Electronic Design (ASQED)*, Aug. 2010, pp. 230-234. DOI: 10.1109/ASQED.2010. 5548244.

Ci24. H. Li and Y. Chen, "Emerging Non-Volatile Memory Technologies – From Materials, to Device, Circuit, and Architecture," *53rd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2010, pp. 1-4. DOI: 10.1109/MWSCAS.2010.5548590.

Ci25. Y. Chen, H. Li, X. Wang, "Spintronic Devices: from Memory to Memristor," *International Conference on Communications, Circuits and Systems (ICCCAS)*, Jul., 2010, pp. 811-816. DOI: 10.1109/ICCCAS.2010. 5581868.

Ci26. X. Wang and Y. Chen, "Spintronic Memristor Devices and Application," *Design, Automation & Test in Europe (DATE)*, Mar. 2010, pp. 667-672. DOI: 10.1109/DATE.2010.5457118.

Ci27. Y. Chen and X. Wang, "Compact Modeling and Corner Analysis of Spintronic Memristor," *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, Jul. 2009, pp. 7-12. DOI: 10.1109/ NANOARCH.2009.5226363.

Ci28. H. Li, and Y. Chen, "An Overview of Non-Volatile Memory Technology and the Implication for Tools and Architectures", *Design, Automation & Test in Europe (DATE)*, Mar. 2009, pp. 731-736. DOI: 10. 1109/DATE.2009.5090761.

VIII. Peer Reviewed Conference Publications (Total: 80)

SINCE SEP. 2010

C1. *J. Guo, *W. Wen, J. Hu, D. Wang, H. Li, and Y. Chen, "FlexLevel: a Novel NAND Flash Storage System Design for LDPC Latency Reduction," *Design Automation Conference (DAC),* Jun. 2015, to appear.

C2. *B. Liu, X. Li, Q. Wu, T. Huang, H. Li, and Y. Chen, "Vortex: Variation-aware Training for Memristor X-bar," *Design Automation Conference (DAC),* Jun. 2015, to appear.

C3. *X. Chen, J. Xue and Y. Chen, "DaTuM: Dynamic Tone Mapping Technique for OLED Display Power Saving based on Video Classification," *Design Automation Conference (DAC),* Jun. 2015, to appear.

C4. *X. Liu, #M. Mao, B. Liu, B. Li, H. Jiang, Y. Wang, M. Barnell, Q. Wu, J. Yang, H. Li, and Y. Chen, "Reno: A Highly-efficient Reconfigurable Neuromorphic Computing Accelerator Design," *Design Automation Conference (DAC),* Jun. 2015, to appear.

C5. #W. Wen, C.-R. Wu, X. Hu, B. Liu, T.-Y. Ho, X. Li, and Y. Chen, "An EDA Framework for Large Scale Hybrid Neuromorphic Computing Systems," *Design Automation Conference (DAC),* Jun. 2015, to appear.

C6. #M. Mao, J. Hu, Y. Chen, and H. Li, "VWS: A Versatile Warp Scheduler for Exploring Diverse Cache Localities of GPGPU Applications," *Design Automation Conference (DAC),* Jun. 2015, to appear.

C7. #C. Liu, *B. Yan, C. Yang, *L. Song, Z. Li, *B. Liu, Q. Wu, H. Jiang, Y. Chen, and H. Li, "A Spiking Neuromorphic Design with Resistive Crossbar," *Design Automation Conference (DAC),* Jun. 2015, to appear.

C8. S. Gu, Q. Zhuge, J. Hu, Y. Chen, and E. Sha, "Area and Performance Co-optimization for Domain Wall Memory in Application-specific Embedded Systems," *Design Automation Conference (DAC),* Jun. 2015, to appear.

C9. Z. Li, *B. Yan, L. Yang, W. Zhao, Y. Chen, and H. Li, "A New Self-reference Sensing Scheme for TLC MRAM," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Jun. 2015, to appear.

C10. T. Tang, L. Xia, B. Li, R. Luo, Y. Wang, Y. Chen, and H. Yang, "Spiking Neural Network with RRAM: Can We Use It for Real-World Application?" *Design, Automation & Test in Europe (DATE)*, Mar. 2015, to appear.

C11. *X. Liu, #M. Mao, X. Bi, H. Li, and Y. Chen, "An Efficient STT-RAM-based Register File in GPU Architectures," *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2015, pp. 490-495. DOI: 10.1109/ASPDAC.2015.7059054.

C12. M. Xie, C. Pan, J. Hu, Y. Chen, and C. Yang, "Checkpoint-aware Instruction Scheduling for Nonvolatile Processor with Multiple Functional Units," *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2015 pp. 316-321. DOI: 10.1109/ASPDAC.2015.7059024.

C13. X. Li, S. Duan, L. Wang, T. Huang, and Y. Chen, "Memristive Radial Basis Function Neural Network for Parameters Adjustment of PID Controller," *International Symposium on Neural Networks (ISNN)*, Nov.-Nov. 2014. Also published on Advances in Neural Networks, Lecture Notes in Computer Science, vol. 8866, pp 150-158. DOI: 10.1007/978-3-319-12436-0_17.

C14. *B. Liu, T. Huang, Q. Wu, M. Barnell, X. Li, and Y. Chen, "Reduction and IR-drop Compensations Techniques for Reliable Neuromorphic Computing," *International Conference on Computer Aided Design (ICCAD),* Nov. 2014, pp. 63-70.

C15. C. Pan, J. Hu, and Y. Chen, "3M-PCM: Exploiting Multiple Write Modes MLC Phase Change Main Memory in Embedded Systems," *International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, article no. 33, Oct. 2014. DOI: 10.1145/2656075.2656076

C16. *X. Liu, #M. Mao, H. Li, Y. Chen, H. Jiang, J. Yang, Q. Wu, and M. Barnell, "A Heterogeneous Computing System with Memristor-based Neuromorphic Accelerators," *IEEE High Performance Extreme Computing Conference (HPEC)*, Sep. 2014, to appear.

C17. C. Zhang, G. Sun, P. Li, T. Wang, D. Niu and Y. Chen, "SBAC: A Statistics based Cache Bypassing Method for Asymmetric-access Caches," *International Symposium on Low Power Electronics and Design (ISLPED)*, Aug. 2014, pp. 345-350. DOI: 10.1145/2627369.2627611.

C18. +X. Hu, G. Feng, H. Li, Y. Chen and S. Duan, "An Adjustable Memristor Model and Its Application in Small-world Neural Networks," *International Joint Conference on Neural Networks (IJCNN)*, Jul. 2014, pp. 7-14. DOI: 10.1109/IJCNN.2014.6889605.

C19. +L. Chen, C. Li, T. Huang, X. He, H. Li and Y. Chen, "STDP Learning Rule Based on Memristor with STDP Property," *International Joint Conference on Neural Networks (IJCNN)*, Jul. 2014, pp. 1-6. DOI: 10.1109/IJCNN.2014.6889506.

C20. #M. Mao, *W. Wen, *Y. Zhang, H. Li, and Y. Chen, "Exploration of GPGPU Register File Architecture Using Domain-wall-shift-write based Racetrack Memory," *Design Automation Conference (DAC)*, Jun. 2014, pp. 1-6. DOI: 10.1145/2593069.2593137.

C21. *W. Wen, #M. Mao, *Y. Zhang, and Y. Chen, "State-Restrict MLC STT-RAM Designs for High-Reliable High-Performance Memory System," *Design Automation Conference (DAC)*, Jun. 2014, pp. 1-6. DOI: 10.1145/2593069.2593220. ***(Best Paper Nomination, 1 out of 42 in track, 2.4%)***

C22. *E. Eken, *Y. Zhang, *W. Wen, R. Joshi, H. Li, and Y. Chen, "A New Field-assisted Access Scheme of STT-RAM with Self-reference Capability," *Design Automation Conference (DAC)*, Jun. 2014, pp. 1-6. DOI: 10.1145/2593069.2593075.

C23. M. Hu, Y. Wang, Q. Qiu, Y. Wang, Y. Chen, and H. Li, "The Stochastic Modeling of TiO2 Memristor and Its Usage in Neuromorphic System Design," *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2014, pp. 831-836. DOI: 10.1109/ASPDAC.2014.6742993.

C24. *J. Guo, *Z. Chen, D. Wang, Z. Shao and Y. Chen, "DPA: Data Pattern Aware Error Prevention Technique to Extend NAND Flash System Lifetime," *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2014, pp. 592-597. DOI: 10.1109/ASPDAC.2014.6742955.

C25. *X. Liu, Y. Li, *Y. Zhang, A. Jones, and Y. Chen, "STD-TLB: A STT-RAM-based Dynamically-configurable Translation Lookaside Buffer for GPU Architectures," *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2014, pp. 355-360. DOI: 10.1109/ASPDAC.2014.6742915.

C26. #M. Mao, G. Sun, Y. Li, A. Jones, and Y. Chen, "Prefetching Techniques for STT-RAM based Last-level Cache in CMP Systems," *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2014, pp. 67-72. DOI: 10.1109/ASPDAC.2014.6742868. ***(Best Paper Nomination, 1 out of 26 in track, 3.8%)***

C27. B. Li, Y. Wang, H. Yang, J. Wong and Y. Chen, "Training Itself: Mixed-signal Training Acceleration for Memristor-based Neural Network," *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2014, pp. 361-366.

C28. *Y. Zhang, *I. Bayram, Y. Wang, H. Li, and Y. Chen, "ADAMS: Asymmetric Differential STT-RAM Cell Structure for Reliable and High-performance Applications," *International Conference on Computer Aided Design (ICCAD)*, Nov. 2013, pp. 9-16. DOI: 10.1109/ICCAD.2013.6691091.

C29. *W. Wen, #M. Mao, S. Kang, X. Zhu, D. Wang and Y. Chen, "CD-ECC: Content-Dependent Error Correction Codes for Combating Asymmetric Nonvolatile Memory Operation Errors," *International Conference on Computer Aided Design (ICCAD)*, Nov. 2013, pp. 1-8. DOI: 10.1109/ICCAD.2013.6691090.

C30. M. Zhao, H. Zhang, *X. Chen, Y. Chen, and J. Xue, "Online OLED Dynamic Voltage Scaling for Video Streaming Applications on Mobile Devices," *International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Oct. 2013, pp. 1-10. DOI: 10.1109/CODES-ISSS.2013.6658996.

C31. *B. Liu, M. Hu, H. Li, Z.-H. Mao, Y. Chen, T. Huang, and W. Zhang, "Digital-Assisted Noise Eliminating Training for Memristor Crossbar-based Analog Neuromorphic Computing Engine," *Design Automation Conference (DAC)*, Jun. 2013, Article 7. DOI: 10.1145/2463209.2488741.

C32. #M. Mao, H. Li, A. Jones, and Y. Chen, "Coordinating Prefetching and STT-RAM-based Last-level Cache Management for Multicore Systems," *Great Lakes Symposium on VLSI (GLVLSI)*, May 2013, pp. 55-60. DOI: 10.1145/2483028.2483060. ***(Best Paper Award)***

C33. M. Hu, H. Li, Y. Chen, Q. Wu, G. S. Rose, "BSB Training Scheme Implementation on Memristor-Based Circuit," *IEEE Symposium on Computational Intelligence for Security and Defense Applications (CISDA)*, Apr. 2013, pp. 80-87. DOI: 10.1109/CISDA.2013.6595431.

C34. *J. Guo, *W. Wen, and Y. Chen, "DA-RAID-5: A Disturb Aware Data Protection Technique for NAND Flash Storage Systems," *Design, Automation & Test in Europe (DATE)*, Mar. 2013, pp. 380-385. DOI: 10.7873/DATE.2013.087.

C35. *J. Guo, J. Yang, Y. Zhang and Y. Chen, "Low Cost Power Failure Protection for MLC NAND Flash Storage Systems with PRAM/DRAM Hybrid Buffer," *Design, Automation & Test in Europe (DATE)*, Mar. 2013, pp. 859-864. DOI: 10.7873/DATE.2013.181.

C36. *X. Chen, Z. Ma, F. C. A. Fernandes, and Y. Chen, "How is Energy Consumed in Smartphone Display Applications," *The International Workshop on Mobile Computing Systems and Applications* (*HotMobile)*, Feb. 2013, Article No. 3. DOI: 10.1145/2444776.2444781. (17 out of 54)

C37. Q. Li, J. Li, L. Shi, C. J. Xue, Y. Chen, and Y. He, "Compiler-Assisted Refresh Minimization for Volatile STT-RAM Cache," *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2013, pp. 273-278. DOI: 10.1109/ASPDAC.2013.6509608. ***(Best Paper Nomination, 1 out of 34 in track, 3%)***

C38. *W. Wen, Y. Zhang, L. Zhang, and Y. Chen, "Loadsa: A Yield-Driven Top-Down Design Method for STT-RAM Array," *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2013, pp. 291-296. DOI: 10.1109/ASPDAC.2013.6509611.

C39. *Y. Zhang, *L. Zhang, *W. Wen, G. Sun and Y. Chen, "Multi-level Cell STT-RAM: Is It Realistic or Just a Dream?" *International Conference on Computer Aided Design (ICCAD)*, Nov. 2012, pp.526-532. DOI: 10.1145/2429384.2429498.

C40. *X. Chen, *B. Liu, Y. Chen, M. Zhao, J. Xue, and X. Guo, "Active Compensation Technique for the Thin-Film Transistor Variations and OLED Aging of Mobile Device Displays," *International Conference on Computer Aided Design (ICCAD)*, Nov. 2012, pp. 516-522. DOI: 10.1145/2429384.2429493.

C41. *P. Wang, W. Zhang, R. Joshi, R. Kanj and Y. Chen, "A Thermal and Process Variation Aware MTJ Switching Model and Its Applications in Soft Error Analysis," *International Conference on Computer Aided Design (ICCAD)*, Nov. 2012, pp.720-727. DOI: 10.1145/2429384.2429541.

C42. *B. Liu, Y. Chen, B. Wysocki, and T. Huang, "The Circuit Realization of a Neuromorphic Computing System with Memristor-based Synapse Design," *International Conference on Neural Information Processing (ICONIP)*, Nov. 2012, pp. 357-365. DOI: 10.1007/978-3-642-34475-6_43. (Published on Neural Information Processing Lecture Notes in Computer Science Volume 7663, 2012)

C43. Y. Li, Y. Chen, and A. K. Jones, "A Software Approach for Combating Asymmetries of Non-Volatile Memories," *International Symposium on Low Power Electronics and Design (ISLPED)*, Jul.-Aug. 2012, pp. 191-196. DOI: 10.1145/2333660.2333708.

C44. G. Sun, *Y. Zhang, Y. Wang, and Y. Chen, "Improving Energy Efficiency of Write-Asymmetric Memories by Log Style Write," *International Symposium on Low Power Electronics and Design (ISLPED)*, Jul.-Aug. 2012, pp. 173-178. DOI: 10.1145/2333660.2333705.

C45. M. Hu, H. Li, Q. Wu, G. S. Rose, and Y. Chen, "Memristor Crossbar Based Hardware Realization of BSB Recall Function," *2012 International Joint Conference on Neural Networks (IJCNN)*, Jun. 2012, pp. 1-7. DOI: 10.1109/IJCNN.2012.6252563.

C46. *W. Wen, *Y. Zhang, Y. Chen, Y. Wang, and Y. Xie, "PS3-RAM: A Fast, Portable and Scalable Statistical STT-RAM Reliability Analysis Method," *Design Automation Conference (DAC)*, Jun. 2012, pp. 1191-1196. DOI: 10.1145/2228360.2228580.

C47. *X. Chen, *J. Zeng, Y. Chen, M. Zhao, and C. J. Xue, "Quality-retaining OLED Dynamic Voltage Scaling for Video Streaming Applications on Mobile Devices," *Design Automation Conference (DAC)*, Jun. 2012, pp. 1000-1005. DOI: 10.1145/2228360.2228540.

C48. *Y. Zhang, X. Wang, Y. Li, A. Jones and Y. Chen, "Asymmetry of MTJ Switching and Its Implication to the STT-RAM Designs," *Design, Automation & Test in Europe (DATE),* Mar. 2012, pp. 1313-1318. DOI: 10.1109/DATE.2012.6176695.

C49. X. Bi, H. Li, Y. Chen, and R. Pino, "Spintronic Memristor Based Temperature Sensor Design with CMOS Current Reference," *Design, Automation & Test in Europe (DATE),* Mar. 2012, pp. 1301-1306. DOI: 10.1109/DATE.2012.6176693.

C50. *X. Chen, J. Zeng, H. Li, W. Zhang, and Y. Chen, "Fine-grained Dynamic Voltage Scaling on OLED Display," *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2012, pp. 807-812. DOI: 10.1109/ASPDAC.2012.6165066.

C51. *Y. Zhang, X. Wang and Y. Chen, "STT-RAM Cell Design Optimization for Persistent and Non-Persistent Error Rate Reduction: A Statistical Design View," *International Conference on Computer Aided Design (ICCAD)*, Nov. 2011, pp. 471-477. DOI: 10.1109/ICCAD.2011.6105370.

C52. Y. Chen, W.-F. Wong, H. Li and C.-K. Koh, "Processor Caches built using Multi-Level Spin-Transfer Torque RAM Cells," *International Symposium on Low Power Electronics and Design (ISLPED)*, Aug. 2011, pp. 73-78. DOI: 10.1109/ISLPED.2011.5993610.

C53. M. Hu, H. Li, Y. Chen, X. Wang, and R. E. Pino, "Geometry Variations Analysis of TiO_2–based and Spintronic Memristors," *16th Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2011, pp. 25-30. DOI: 10.1109/ASPDAC.2011.5722193. ***(Best Paper Nomination, 1 out of 28 in track, 3.6%)***

C54. Z. Sun, H. Li, Y. Chen, and X. Wang, "Variation Tolerant Sensing Scheme of Spin-Transfer Torque Memory for Yield Improvement," *International Conference on Computer Aided Design (ICCAD)*, Nov. 2010, pp. 432-437. DOI: 10.1109/ICCAD.2010.5653720.

<u>BEFORE SEP. 2010</u>

C55. D. Niu, Y. Chen, and Y. Xie, "Low-power Dual-element Memristor-Based Memory Design," *International Symposium on Low Power Electronics and Design (ISLPED)*, Aug. 2010, pp. 25-30. DOI: 10.1145/1840845.1840851.

C56. Y. Chen, H. Li, X. Wang, W. Zhu, W. Xu and T. Zhang, "Combined Magnetic- and Circuit-level Enhancements for the Nondestructive Self-Reference Scheme of STT-RAM," *International Symposium on Low Power Electronics and Design (ISLPED)*, Aug. 2010, pp. 1-6. DOI: 10.1145/1840845.1840847. ***(Best Paper Award, 2 out of 300, 0.67%)***.

C57. Y. Chen, H. Li, Z. Sun, X. Wang, W. Zhu, G. Sun and Y. Xie, "Access Scheme of Multi-Level Cell Spin-Transfer Torque Random Access Memory and Its Optimization," *53rd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2010, pp.1109-1112. DOI: 10.1109/MWSCAS.2010.5548848.

C58. D. Niu, Y. Chen, C. Xu, and Y. Xie, "Impact of Process Variations on Emerging Memristor," *Design Automation Conference (DAC)*, Jun. 2010, pp. 877-882. DOI: 10.1145/1837274.1837495.

C59. Y. Chen, W. Tian, H. Li, X. Wang, and W. Zhu, "Scalability of PCMO-based Resistive Switch Device in DSM Technologies," *International Symposium on Quality Electronic Design (ISQED),* Mar. 2010, pp. 327-332. DOI: 10.1109/ISQED.2010.5450447. ***(Best Paper Nomination, 9 out of 245, 3.7%).***

C60. Y. Chen, H. Li, X. Wang, W. Zhu, W. Xu, and T. Zhang, "A Nondestructive Self-Reference Scheme for Spin-Transfer Torque Random Access Memory (STT-RAM)," *Design, Automation & Test in Europe*

(DATE), Mar. 2010, pp. 148-153. DOI: 10.1109/DATE.2010.5457219. ***(Best Paper Nomination, 20 out of 981, 2.0%)***

C61. G. Sun, Y. Joo, Y. Chen, Y. Xie, Y. Chen, and H. Li, "A Hybrid Solid-State Storage Architecture for the Performance, Energy Consumption, and Lifetime Improvement," *International Symposium on High-Performance Computer Architecture (HPCA)*, Jan. 2010, pp. 141-152. DOI: 10.1109/HPCA.2010.5416650.

C62. C.-K. Koh, W.-F. Wong, Y. Chen, and H. Li, "The Salvage Cache: A Fault-tolerant Cache Architecture for Next-generation Memory Technologies," *International Conference on Computer Design (ICCD)*, Oct. 2009, pp.268-274. DOI: 10.1109/ICCD.2009.5413145.

C63. W. Xu, Y. Chen, X. Wang, and T. Zhang, "Improving STT MRAM Storage Density through Smaller-Than-Worst-Case Transistor Sizing," *Design Automation Conference (DAC)*, Jul. 2009, pp. 87-90. DOI: 10.1145/1629911.1629936.

C64. H. Li, H. Xi, Y. Chen, J. Stricklin, X. Wang, and T. Zhang, "Thermal-Assisted Spin Transfer Torque Memory (STT-RAM) Cell Design Exploration," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI),* May 2009, pp. 217-222. DOI: 10.1109/ISVLSI.2009.17.

C65. G. Sun, X. Dong, Y. Xie, J. Li, and Y. Chen, "A Novel Architecture of the 3D Stacked MRAM L2 Cache for CMPs," *14th International Symposium on High-Performance Computer Architecture (HPCA)*, Feb. 2009, pp. 239-249. DOI: 10.1109/HPCA.2009.4798259.

C66. X. Dong, X. Wu, G. Sun, Y. Xie, Y. Chen, and H. Li, "Circuit and Microarchitecture Evaluation of 3D Stacking Magnetic RAM (MRAM) as a Universal Memory Replacement," *Design Automation Conference (DAC)*, Jun. 2008, pp. 554-559. DOI: 10.1145/1391469.1391610.

C67. W. Xu, T. Zhang and Y. Chen, "Spin-Transfer Torque Magnetoresistive Content Addressable Memory (CAM) Cell Structure Design with Enhanced Search Noise Margin," *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2008, pp. 1898-1901. DOI: 10.1109/ISCAS.2008.4541813.

C68. Y. Chen, X. Wang, H. Li, H. Liu and D. Dimitrov, "Design Margin Exploration of Spin-Torque Transfer RAM (SPRAM)," *International Symposium on Quality Electronic Design (ISQED)*, Mar. 2008, pp. 684-690. DOI: 10.1109/ISQED.2008.4479820. ***(Best Paper Award, 3 out of 300 submissions, 1%)***

C69. C.-K. Koh, W.-F. Wong, Y. Chen, and H. Li, "VOSCH: Voltage Scaled Cache Hierarchies," *International Conference on Computer Design (ICCD)*, Oct. 2007, pp. 496-503. DOI: 10.1109/ICCD.2007.4601944.

C70. Y. Chen, H. Li, J. Li and C.-K. Koh, "Variable-latency Adder (VL-Adder): New Arithmetic Circuit Design Practice to Overcome NBTI," *International Symposium on Low Power Electronics and Design (ISLPED)*, Aug. 2007, pp. 195-200. DOI: 10.1145/1283780.1283822.

C71. H. Li, C.-K. Koh, V. Balakrishnan and Y. Chen, "Statistical Timing Analysis Considering Spatial Correlations," *International Symposium on Quality Electronic Design (ISQED)*, Mar. 2007, pp. 102-107. DOI: 10.1109/ISQED.2007.149.

C72. H. Li, Y. Chen, K. Roy and C.-K. Koh, "SAVS: A Self-adaptive Variable Supply-voltage Technique for Process-tolerant and Power-efficient Multi-issue Superscalar Processor Design," *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2006, pp. 158-163. DOI: 10.1109/ASPDAC.2006.1594675.

C73. W.-C. D. Lam, J. Jain, C.-K. Koh, V. Balakrishnan and Y. Chen, "Statistical Based Link Insertion for Robust Clock Network Design," *International Conference on Computer-Aided Design (ICCAD)*, Nov. 2005, pp. 588-591. DOI: 10.1109/ICCAD.2005.1560134.

C74. Y. Chen, H. Li, K. Roy and C.-K. Koh, "Gated Decap: Gate Leakage Control of On-chip Decoupling Capacitors in Scaled Technologies," *IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2005, pp. 775-778. DOI: 10.1109/CICC.2005.1568783.

C75. D. Kung, Y. Chen, and K. Roy, "Power Supply Noise-aware Scheduling and Allocation for DSP Synthesis," *International Symposium on Quality Electronic Design (ISQED)*, Mar. 2005, pp. 48-53. DOI: 10.1109/ISQED.2005.97. ***(Best Paper Nomination, 9 out of 222 submissions, 4.1%)***

C76. Y. Chen, K. Roy and C.-K. Koh, "Priority Assignment Optimization for Minimization of Current Surge in High Performance Power Efficient Clock-gated Microprocessor," *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2004, pp. 893-898. DOI: 10.1109/ASPDAC.2004.1337722.

C77. Y. Chen, K. Roy and C.-K. Koh, "Integrated Architectural/Physical Planning Approach for Minimization of Current Surge in High Performance Clock-gated Microprocessors," *International Symposium on Low Power Electronics and Design (ISLPED)*, Aug. 2003, pp. 229-234. DOI: 10.1109/LPE.2003.1231867.

C78. H. Li, S. Bhunia, Y. Chen, T.N.Vijaykumar, and K. Roy, "Deterministic Clock Gating for Microprocessor Power Reduction," *International Symposium on High-Performance Computer Architecture (HPCA)*, Feb. 2003, pp. 113-122. DOI: 10.1109/HPCA.2003.1183529.

C79. Y. Chen, V. Balakrishnan, C.-K. Koh and K. Roy, "Model Reduction in the Time-domain using Laguerre Polynomials and Krylov Methods," *Design, Automation & Test in Europe (DATE)*, Mar. 2002, pp. 931-937. DOI: 10.1109/DATE.2002.998411.

C80. Y. Chen, L. Zhang, Z. Jiang, Q. Yu and C. Fan, "Suppression of Stimulated Brillouin Scattering induced by the Compensating Signal in All-Optical Gain-Clamped EDFA," *International Conference on Communication Technology (ICCT)*, 2000, pp. 203-205. DOI: 10.1109/ICCT.2000.889198.

IX. Peer Reviewed Conference Posters, Presentations, Tracks of Working-in-progress (WIP) and Interactive Presentations (IP) (Total: 15)

SINCE SEP. 2010

In Proceeding

Cp1. Y. Wang, B. Li, R. Luo and Y. Chen, "Energy Efficient Neural Networks for Big Data Analytics," *Design, Automation & Test in Europe (DATE)*, Mar. 2014, 1-2. DOI: 10.7873/DATE.2014.358.

Cp2. B. Li, Y. Wang, Y. Chen, H. Li, and H. Yang, "ICE: Inline Calibration for Memristor Crossbar-based Computing Engine," *Design, Automation & Test in Europe (DATE)*, Mar. 2014, 1-4. DOI: 10.7873/DATE.2014.197.

Cp3. J. Li, L. Shi, Q. Li, C. J. Xue, Y. Chen, and Y. Xu, "Cache Coherence Enabled Adaptive Refresh for Volatile STT-RAM," *Design, Automation & Test in Europe (DATE)*, Mar. 2013, pp. 1247-1250. DOI: 10.7873/DATE.2013.258.

Cp4. B. Zhao, J. Yang, Y. Zhang, Y. Chen and H. Li, "Architecting a Common-Source-Line Array for Bipolar Non-Volatile Memory Devices," *Design, Automation & Test in Europe (DATE)*, March 2012, pp. 1451-1454. DOI: 10.1109/DATE.2012.6176594.

Cp5. *P. Wang, X. Chen, Y. Chen, H. Li, S. Kang, X. Zhu, and W. Wu, "A 1.0V 45nm Nonvolatile Magnetic Latch Design and Its Robustness Analysis," *IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2011, pp.1-4. DOI: 10.1109/CICC.2011.6055392.

Cp6. P. Zhou, B. Zhao, J. Yang, Y. Zhang, and Y. Chen, "MRAC: A Memristor-based Reconfigurable Framework for Adaptive Cache Replacement," *International conference on Parallel Architectures and Compilation Techniques (PACT)*, Sep. 2011, pp. 207-208. DOI: 10.1109/PACT.2011.29.

Cp7. Y.-C. Chen, H. Li, Y. Chen and R. Pino, "3D-ICML: A 3D Bipolar ReRAM Design with Interleaved Complementary Memory," *Design, Automation & Test in Europe (DATE)*, Mar. 2011, pp. 1-4. DOI: 10.1109/DATE.2011.5763289.

No Proceeding

Cp8. X. Zhang, G. Sun, *Y. Zhang, *W. Wen, Y. Chen, and J. Di, "err-PUF: Exploiting Cell Error Distribution for Secure NVM Authentication," *Design Automation Conference (DAC),* Jun. 2015.

Cp9. *B. Liu, M. Barnell, Q. Wu, T. Huang, X. Li, and Y. Chen, "Model Reduction and IR-drop Compensations Techniques for Reliable Neuromorphic Computing Systems," *Design Automation Conference (DAC)*, Jun. 2014.

Cp10. K. Li, D. Gray-Miceli, C. Or, Z. Li, Y. Chen and S. Zhang, "Human Airbags for Falls and Injury Prevention," *HFES 2014 International Symposium on Human Factors and Ergonomics in Health Care: Leading the Way*, Mar. 2014. (Presentation)

Cp11. *X. Chen, Y. Chen, Z. Ma, F. Fernandes, and J. Xue, "Dynamic Tone Mapping on OLED Display Based on Video Classification," *50th Design Automation Conference (DAC)*, Jun. 2013.

Cp12. *K. Nixon, *X. Chen, Z.-H. Mao, K. Li, and Y. Chen, "The Invisible Shield: User Classification and Authentication for Mobile Device Based on Gesture Recognition," *Design Automation Conference (DAC)*, Jun. 2013.

Cp13. L. Niu, L. Medina and Y. Chen, "Reliability-Aware Energy Minimization for Real-Time Embedded Systems with Window-Constraints," *IEEE Real-Time Systems Symposium (RTSS)*, Dec. 2012.

Cp14. M. Zhao, X. Chen, Y. Chen and J. Xue, "Online OLED Dynamic Voltage Scaling for Video Streaming Applications on Mobile Devices," *IEEE Real-Time Systems Symposium (RTSS)*, Dec. 2012.

Cp15. M. Hu, H. Li, Y. Chen, and R. E. Pino, "Statistical Model of TiO_2 Memristor," *48th Design Automation Conference (DAC)*, June 2011.

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Cp16. Y. Chen, H. Li, K. Roy and C.-K. Koh, "Cascaded Carry-Select Adder (C^2SA): A New Structure for Low-Power CSA Design," *International Symposium on Low Power Electronics and Design (ISLPED)*, Aug. 2005, pp. 115-118. DOI: 10.1109/LPE.2005.195498. (In proceeding)

X. Peer Reviewed Conference Abstracts and Workshop Publications (Total: 23)

SINCE SEP. 2010

Cw1. *E. Eken, Y. Zhang, B. Yan, W. Wen, H. Li, and Y. Chen, "Spin-Hall Assisted STT-RAM Design and Discussion," *IEEE International Magnetics Conference (InterMag)*, May 2015, BB-02.

Cw2. H. Li, B. Liu, X. Liu, M. Mao, Y. Chen, Q. Wu, and Q. Qiu, "The Applications of Memristor Devices in Next-generation Cortical Processor Designs," *International Workshop on Neuromorphic and Brain-Based Computing Systems (NeuComp)*, Mar. 2015. (Poster)

Cw3. *B. Liu, T. Huang, Q. Wu, M. Barnell, X. Li, and Y. Chen, "Reduction and IR-drop Compensations Techniques for Reliable Neuromorphic Computing," *International Workshop on Design Automation for Analog and Mixed-Signal Circuits*, Nov. 2014. (Poster)

Cw4. *K. Nixon, *X. Chen, H. Zhou, Y. Liu and Y. Chen, "Mobile GPU Power Consumption Reduction via Dynamic Resolution and Frame Rate Scaling," *Workshop on Power-Aware Computing and Systems (HotPower)*, Oct. 2014. (9 out of 26)

Cw5. *X. Chen, *K. Nixon, H. Zhou, Y. Liu, and Y. Chen, "FingerShadow: An OLED Power Optimization based on Smartphone Touch Interactions," *Workshop on Power-Aware Computing and Systems (HotPower)*, Oct. 2014, to appear. (9 out of 26)

Cw6. *E. Eken, Y. Zhang, W. Wen, R. Joshi, H. Li, and Y. Chen, "A New Field-assisted Access Scheme of STT-RAM with Self-reference Capability," *IEEE International Magnetics Conference (InterMag)*, May 2014, CC-09.

Cw7. *Y. Zhang, *I. Bayram, Y. Wang, H. Li and Y. Chen, "ADAMS: Asymmetric Differential STT-RAM Cell Structure for Reliable and High-performance Applications," *International Workshop on Design Automation for Analog and Mixed-Signal Circuits*, Nov. 2013. (Poster)

Cw8. #M. Mao, G. Sun, Y. Li, A. Jones, and Y. Chen, "Prefetching Techniques for STT-RAM based Last-level Cache in CMP Systems," *Memory Architecture and Organization Workshop (MeoAW)*, Oct. 2013.

Cw9. *B. Liu, M. Hu, H. Li, Y. Chen, and J. Xue, "Bio-Inspired Ultra Lower-Power Neuromorphic Computing Engine for Embedded Systems," *International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Oct. 2013, to appear. (invited, in proceeding)

Cw10. M. Hu, H. Li, G. Rose, Q. Wu and Y. Chen, "Training Scheme Analysis for Memristor-Based Neuromorphic Design," *International Workshop on Neuromorphic and Brain-Based Computing Systems (NeuComp)*, Mar. 2013.

Cw11. #M. Mao, H. Li, A. Jones, J. Xue, and Y. Chen, "Dynamic Prefetch Aggressiveness Tuning for STT-RAM-based Last-level Cache," *4th Workshop on SoCs, Heterogeneous Architectures and Workloads (SHAW4)*, Feb. 2013.

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22. "The Applications of Emerging Devices in Future On-chip and Off-chip Storage Systems," Strategy and Technology Workshop (STW), Huawei, Shenzhen, China, May 14, 2014.
23. "Emerging Nonvolatile Memories Designs and Applications in Conventional & Neuromorphic Computing," Beihang University, Beijing, China, Apr. 26, 2014.
24. "Emerging Nonvolatile Memories Designs and Applications in Conventional & Neuromorphic Computing," Ming Hsieh Department of Electrical Engineering, University of Southern California Los Angeles, CA, Apr. 2, 2014.
25. "Next-generation Nonvolatile Memory Technologies: Design Space Exploration and Applications in Modern Computing Systems," *Advanced Digital Sciences Center*, Singapore, Jan. 24, 2014.
26. "MRAM Design and Optimization: Challenges and Opportunities," *Nanjing University*, Nanjing, China, Dec. 16, 2013.
27. "Next-generation Nonvolatile Memory Technologies: Design Space Exploration and Applications in Modern Computing Systems," *National Cheng Kung University*, Tainan, Taiwan, Nov. 28, 2013.
28. "Next-generation Nonvolatile Memory Technologies: Design Space Exploration and Applications in Modern Computing Systems," *Apple*, Cupertino, CA, Oct. 25, 2013.
29. "The Invisible Shield: User Classification and Authentication for Mobile Device Based on Gesture Recognition," *Qualcomm*, Santa Clara, CA, Oct. 25, 2013.
30. "Next-generation Nonvolatile Memory Technologies: Design Space Exploration and Applications in Conventional and Neuromorphic Computing," *Guangzhou Institute of Advanced Technology*, *China Academy of Science*, Guangzhou, China, Oct. 16, 2013.
31. "System-Level Consideration for STT-RAM Designs," *HUAWEI Storage Day*, Shenzhen, China, Oct. 15, 2013.
32. "Next-generation Nonvolatile Memory Technologies: Design Space Exploration and Applications in Conventional and Neuromorphic Computing," *IBM Thomas J Watson Research Center*, Yorktown Heights, NY, Aug. 16, 2013.
33. "Centaur: Bio-inspired Ultra Low-Power Hybrid Embedded Computing Engine Beyond One TeraFlops/Watt," *5th International Workshop on Emerging Circuits and Systems (IWECS)*, Chengdu, China, Jul. 25, 2013.
34. "Prediction of STT-RAM Parameters for 2012-2025," *Cloud·Storage·Big Data Summit jointly held with the 2nd Asian Nonvolatile Memory Workshop (ANVMW)*, Shanghai, China, Jul. 22, 2013.
35. "Next-generation Nonvolatile Memory Technologies: Design Space Exploration and Applications in Conventional and Neuromorphic Computing," *Microsoft Research Asia*, Beijing, China, May 23, 2013.
36. "Design space exploration of STT-RAM cells," Spintronics based Computing Workshop, *Beihang University*, Beijing, China, May 22, 2013.
37. "Next-generation Nonvolatile Memory Technologies: Design Space Exploration and Applications in Conventional and Neuromorphic Computing," *EMC Research*, COE Tech Talk Series, Beijing, China, May 21, 2013.
38. "Centaur: Bio-inspired Ultra Low-Power Hybrid Embedded Computing Engine Beyond One TeraFlops/Watt," *Chongqing University*, Chongqing, China, Mar. 13, 2013.
39. "Centaur: Bio-inspired Ultra Low-Power Hybrid Embedded Computing Engine Beyond One TeraFlops/Watt," *Southwest University*, Chongqing, China, Mar. 12, 2013.
40. "Centaur: Bio-inspired Ultra Low-Power Hybrid Embedded Computing Engine Beyond One TeraFlops/Watt," *Hong Kong Polytechnic University*, Hong Kong, Mar. 1, 2013.
41. "Centaur: Bio-inspired Ultra Low-Power Hybrid Embedded Computing Engine Beyond One TeraFlops/Watt," C*ity University of Hong Kong*, Hong Kong, Mar. 1, 2013.
42. "Centaur: Bio-inspired Ultra Low-Power Hybrid Embedded Computing Engine Beyond One TeraFlops/Watt," C*hinese University of Hong Kong*, Hong Kong, Feb. 28, 2013.
43. "Research on NAND Flash Based Storage System Reliability Enhancement," *Fusion-io Inc.*, San Jose, CA, Dec. 11, 2012.

44. "Centaur: Bio-inspired Ultra Low-Power Hybrid Embedded Computing Engine Beyond One TeraFlops/Watt," *International Conference on Neural Information Processing (ICONIP)*, Doha, Qatar, Nov. 13, 2012.
45. "User Classification and Authorization Based on Gesture Usage Recognition," *Network Science and Reconfigurable Systems for Cybersecurity (NSRSC) Conference*, Washington D.C., Aug. 28, 2012.
46. "The Applications of Spintronic Memory in Microprocessors," *Flash Memory Summit*, Santa Clara, CA, Aug. 23, 2012.
47. "Emerging NVM Enabled Computing Architecture – From Evolution to Revolution," *Institute of Computing Technology, Chinese Academy of Sciences*, Jul. 27, 2012.
48. "Prediction of STT-RAM Parameters for 2012-2025," *ERD Workshop on Emerging Architectures for Storage Class Memory*, Monterey, CA, Jul. 8, 2012.
49. "STT-RAM Research of Pitts and NYU-Poly Team," *Samsung*, Dongtan, Korea, Jul. 6, 2012. (Together with Prof. Hai (Helen) Li, NYU)
50. "Stay Spinning, Stay Cool!" *Electronic Engineering Department, Tsinghua University*, Beijing, China, Jun. 29, 2012.
51. "Stay Spinning, Stay Cool!" *Information Engineering School, Zhengzhou University*, Henan, China, Jun. 18, 2012.
52. "Perspective of Nonvolatile Memories in SoC and Computing Systems," *Lenovo Corporate Research and Development*, Beijing, China, Jun. 21, 2012. (Together with Prof. Hai (Helen) Li, NYU)
53. "Introduction to Development of Android Smartphone Applications (Apps)," *U.S. Air Force Research Lab*, Rome, NY, May 17 and 24, 2012.
54. "Stay Spinning, Stay Cool!" *Departmental Colloquium, Department of Electrical & Computer Engineering, University of Pittsburgh, Pittsburgh*, Apr. 17, 2012.
55. "Emerging NVM Enabled Computing Architecture - From Evolution to Revolution," *8th Annual Full Day Symposium Emerging Non-Volatile Memory Technologies*, hosted by IEEE San Francisco Bay Area Nanotechnology Council Chapter, Santa Clara, CA, Apr. 6, 2012.
56. "Emerging Applications of Next-generation Nonvolatile Memory Technologies," *University Relationship Colloquium, Qualcomm Inc.,* San Diego, Mar. 7, 2012.
57. "The Applications of STT-RAM in Microarchitecture," *Institute of Computing Technology, Chinese Academy of Sciences*, Aug. 25, 2011.
58. "STT-RAM Research of University of Pittsburgh Poly-New York University Team," *Avalanche Technology, Fremont*, CA, Aug. 5, 2011. (Together with Prof. Hai (Helen) Li, NYU)
59. Panelist, *2011 Silicon-Valley Magnetic Symposium*, San Jose, June 18, 2011.
60. "Current Research and Its Trend of Emerging Memory Technologies," *The CCF Advanced Disciplines Lectures*, Hangzhou, China, May 8, 2011 and *Hong Kong Polytechnic University*, Hong Kong, May 10, 2011.
61. "Integrating Emerging Memory atop CMP: Opportunities and Challenges from a Designer Perspective," *3D Integration Workshop For High Performance Computing Systems*, Abu Dhabi, United Arab Emirates, Apr. 18, 2011.
62. "Spintronic Memristor: Intelligent Device for Storing, Sensing and Computing," *Spintronic Workshop, Qualcomm Inc.,* San Diego, Mar. 9, 2011.
63. "Resistive Memory and Systems," *Mircoelectronic Institute, Tsinghua University*, Feb. 25, 2011.
64. "A Frank Conversation between a Device Engineer and An Architect: Case Studies in STT-RAM Research," *Workshop on Technology-Architecture Interaction: Emerging Technologies and their Impact on Computer Architecture* (Held in conjunction with 43rd Annual IEEE/ACM International Symposium on Microarchitecture), Atlanta, Dec. 5, 2010.
65. "Applications of Emerging Memory in Modern Computer Architecture," *School of Computing, National University of Singapore, and Nanyang Technology University*, Aug. 3, 2010.
66. "Spintronic devices − An Alternative Path to Continue Moore's Law," *Dalian Mini-Colloquia of IEEE Electron Device Society*, Dalian, China, Jun. 10-11, 2010.

67. "Emerging Resistive Device - an Alternative Path to Continue Moore's Law," CSE Seminar Series, *Department of Computer Science and Engineering, Notre Dame University*, Notre Dame, IN, Mar. 18, 2010.
68. "Emerging Resistive Memory - the Next Breakthrough in Computing System," *Department of Computer Science and Engineering's Colloquium, Pennsylvania State University*, State College, PA, Apr. 8, 2009.
69. "Emerging Non-volatile Memory: Spin-Transfer Torque Memory and Resistive Memory," *Department of Electronic Engineering, Tsinghua University*, Beijing, China, Oct. 22, 2008.
70. "Emerging Non-volatile Memory: Spin-Transfer Torque Memory and Resistive Memory," *Department of Electrical and Computer Engineering's Colloquium, University of Minnesota*, Minneapolis, MN, Oct. 16, 2008.
71. "Resources Balancing: A Technique for Minimization of Current Surge in Microprocessor," *7th SIGDA Ph.D. Forum at Design Automation Conference*, San Diego, CA, Jun. 8, 2004.
72. "Low Power CPU Design," *Institute of Computing Technology, Chinese Academy of Sciences*, Sep. 3, 2003.
73. "System Level Low Power CPU Design," *Department of Electronic Engineering, Tsinghua University*, Aug. 27, 2003.

MEDIA INERVIEW

Featured Engineer, www.eeweb.com, on April 6, 2015.

"Pushing the PRAM: when chips just can't get any smaller", by Jeremy Wagstaff, Reuters, on June 7, 2012.

"Spintronic Memristors", by Neil Savage, IEEE Spectrum, March 16, 2009. (March 2009 Feature Articles)

TEACHING ACTIVITIES

I. Teaching Certification

The College Teaching Workshops, Purdue, 2003 (A 15-hour professional teaching training designed to improve the teaching skills of Purdue faculty, staff, and selected graduate students.)

II. Teaching History

University of Pittsburgh, Electrical & Computer Engineering Department

Note: The teaching evaluation scores are included below. The highest score is 5. The enrollment number may be different from other records due to the different cut off time.

ECE2140: Systems-on-a-Chip Design	Spring 2015	(4.15 out of 5.0)
26 graduate students		
ECE1161/2161: Embedded Computer System Design II	Spring 2015	(4.13 out of 5.0)
22 graduate students and 3 undergraduate students		
ECE1160/2160: Introduction to Embedded Systems.	Fall 2014	(4.17 out of 5.0)
17 graduate students and 17 undergraduate students		
ECE2120: Hardware Design Methodologies	Spring 2014	(4.33 out of 5.0)
25 graduate students		
ECE3195: Emerging Memory and Computer Architecture	Spring 2014	(4.71 out of 5.0)
9 graduate students		
ECE1160/2160: Introduction to Embedded Systems.	Fall 2013	(3.92 out of 5.0)
18 graduate students and 15 undergraduate students		
ECE3195: Emerging Memory and Computer Architecture	Spring 2013	(4.79 out of 5.0)
28 graduate students		
ECE1161/2161: Embedded Computer System Design II	Spring 2013	(4.43 out of 5.0)
15 graduate students and 8 undergraduate students		
ECE1160/2160: Introduction to Embedded Systems.	Fall 2012	(3.94 out of 5.0)
20 graduate students and 14 undergraduate students		
ECE1161/2161: Embedded Computer System Design II	Spring 2012	(4.10 out of 5.0)

24 graduate students and 3 undergraduate students		
ECE1160/2160: Introduction to Embedded Systems.	Fall 2011	(3.73 out of 5.0)
20 graduate students and 16 undergraduate students		
ECE1238: Digital Electronics.	Spring 2011	(3.38 out of 5.0)
19 undergraduate students		
ECE1160/2160: Introduction to Embedded Systems.	Fall 2010	(3.62 out of 5.0)
17 graduate students and 14 undergraduate students		

III. Other teaching activities and achievements:

The first Youtube channel (www.youtube.com/user/PittEmbeddedSystem) is created for embedded system education in Pitt Engineering School. This Youtube channel has been well received by the students in Pitt as well as other external audiences, e.g., the researchers in Air Force Research Lab (AFRL). The up-to-date video reviews are 9906 (on 05/05/2015) and has been subscribed by 56 viewers.

IV. Supervised students as primary adviser (* indicates the students co-supervised with Prof. Hai Li. + indicates the students co-supervised with Prof. Zhi-Hong Mao).

Yaojun Zhang	Ph.D.,	University of Pittsburgh,	2010.09-2014.12(expected)
Xiang Chen	Ph.D.,	University of Pittsburgh,	2011.04-2014.12(expected)
Wujie Wen	Ph.D.,	University of Pittsburgh,	2011.09-2015.07(expected)
Jie Guo	Ph.D.,	University of Pittsburgh,	2011.09-2015.07(expected)
Lu Zhang	Ph.D.,	University of Pittsburgh,	2011.11-2015.12(expected)
Beiye Liu	Ph.D.,	University of Pittsburgh,	2011.12-2015.12(expected)
Xiaoxiao Liu	Ph.D.,	University of Pittsburgh,	2013.01-2017.01(expected)
Kent Nixon	Ph.D.,	University of Pittsburgh,	2013.09-2018.04(expected)
Enes Eken	Ph.D.,	University of Pittsburgh,	2013.09-2017.08(expected)
Bonan Yan	Ph.D.,	University of Pittsburgh,	2014.09-2019.04(expected)
Linghao Song	Ph.D.,	University of Pittsburgh,	2014.09-2019.04(expected)
Abdulkaim Alorf	Ph.D.,	University of Pittsburgh,	2015.01-2019.12(expected)
Chuhan Min	Ph.D.,	University of Pittsburgh,	2015.01-2019.12(expected)
*Ismail Bayram	Ph.D.,	University of Pittsburgh,	2013.01-2017.07(expected)
*Mengjie Mao	Ph.D.,	University of Pittsburgh,	2012.09-2016.07(expected)
*Xue Wang	Ph.D.,	University of Pittsburgh,	2014.01-2019.01(expected)
+Ahmed Dallal	Ph.D.,	University of Pittsburgh,	2013.09-2018.05(expected)
Peiyuan Wang	M.S.,	University of Pittsburgh,	2010.09-2011.12(first job: Qualcomm Res.)
Mumen H. Ramadan	M.S.,	University of Pittsburgh,	2010.11-2013.04(first job: Highmark)
Noah Robin	M.S.,	University of Pittsburgh,	2010.12-2012.04
Jian Zeng	M.S.,	University of Pittsburgh,	2011.05-2011.12(first job: Qualcomm)
Yue Xu	M.S.,	University of Pittsburgh,	2011.09-
Juluri Ramana Naga Shishir	M.S.,	University of Pittsburgh,	2011.09-2013.04(first job: NetApp)
Hexuyuan Chen	M.S.,	University of Pittsburgh,	2012.09-
Xinchao Lu	M.S.,	University of Pittsburgh,	2012.09-
Zhen Liu	M.S.,	University of Pittsburgh,	2012.09-
Enes Eken	M.S.,	University of Pittsburgh,	2013.09-2014.04(first job: Ph.D. at Ph.D.)
Ping Lang	M.S.,	University of Pittsburgh,	2012.09-
Kent Nixon	Under,	University of Pittsburgh,	2012.05-2013.04(continue Ph.D. in Pitt)

V. Dissertation Committees

Jing Li	Ph.D.,	Purdue University,	2007.09-2009.07(first job: IBM Res.)
Dong Jiao	Ph.D.,	University of Minnesota,	2009.09-2011.07(first job: Samsung Res.)
Siwapon Srisonphan	Ph.D.,	University of Pittsburgh,	2010.12-

Vyasa Sai	Ph.D.,	University of Pittsburgh,	2011.02-2013.03
Yi Xu	Ph.D.,	University of Pittsburgh,	2011.05-2012.12(first job: AMD Res.)
David Perello	Ph.D.,	University of Pittsburgh,	2011.05-2013.04
Benjamin W. McMillen	Ph.D.,	University of Pittsburgh,	2011.12-2012.07
Yong Li	Ph.D.,	University of Pittsburgh,	2012.11-2013.12(first job: VMware)
Zhenyu Sun	Ph.D.,	University of Pittsburgh,	2013.04-2013.12(first job: Broadcom)
Xiuyuan Bi	Ph.D.,	University of Pittsburgh,	2013.04-
Miao Hu	Ph.D.,	University of Pittsburgh,	2013.04-
Yi-Chung Chen	Ph.D.,	University of Pittsburgh,	2013.04-
Miao Zhou	Ph.D.,	University of Pittsburgh,	2013.09-2015.05
Haifeng Xu	Ph.D.,	University of Pittsburgh,	2012.04-
Rakan Maddah	Ph.D.,	University of Pittsburgh,	2014.03-2015.05(first job: Intel)
Qin-Hao Zhang	Ph.D.,	University of Pittsburgh,	2014.09-
Shama Huda	M.S.,	University of Pittsburgh,	2011.11-2011.12
Jinxuan Wu	M.S.,	University of Pittsburgh,	2012.03-2012.04
Haifeng Xu	M.S.,	University of Pittsburgh,	2012.03-2012.04 (Continue Ph.D. in Pitt)
Yan Fang	M.S.,	University of Pittsburgh,	2013.04-2013.04 (Continue Ph.D. in Pitt)

V. Visiting Students

Kai Bu	Ph.D.,	NUDT, China	2012.08-2013.01, 2013.07-2013.12
Ling Chen	Ph.D.,	Chongqing Univ., China	2013.09-2014.08

VI. Visiting Professors

Yiguang Gong	Assi P.,	Nanjing Univ. of Info. Sci. & Tech.	2014.10-2015.12
Linan Li	Asso P.,	Beijing Jiaotong University, China	2014.09-2015.08
Lusheng Zhong	Asso P.,	East China Jiaotong University, China	2013.09-2014.08
Danghui Wang	Asso P.,	Northwestern PolyTech University, China	2012.09-2013.08

VII. Personal Teaching Online Resources

Youtube channel of Pitt's embedded system education: http://www.youtube.com/user/pittembeddedsystem.

STUDENT AWARDS/GRANTS

1. Wujie Wen, Travel grant ($650) for Ph.D. Forum at DAC 2015.
2. Xiang Chen, Most Popular Poster, ACM SIGDA Student Research Forum at ASP-DAC 2015.
3. Xiang Chen, Travel grant ($450) for Student Research Forum at ASP-DAC 2015.
4. **Wujie Wen, Bronze Medal of ACM Student Research Competition at ICCAD 2014.**
5. Wujie Wen, Travel grant ($500) for ACM Student Research Competition at ICCAD 2014.
6. Wujie Wen, Dean's fellowship ($1500), 2014.
7. **Kent Nixon, 2nd Place, 3 Rivers Venture Fair University Technology Showplace ($1,500), 2014.**
8. Kent Nixon, EGSO Outstanding Teaching Assistant Award in ECE Department for the 2013-2014 Year.
9. Xiang Chen, the Award of Excellence for 2014 Microsoft Research Asia Internship Program.
10. Yaojun Zhang, Travel grant ($500) for Ph.D. Forum at DAC 2014.
11. Xiaoxiao Liu, A. Richard Newton Young Fellow Program ($1340) for DAC 2014.
12. **Invisible Shield (Kent Nixon and Xiang Chen), Second Prize, Randall Family Big Idea Competition ($4,500), 2014.**
13. KoalaKollar, Grand Competition of Cornell Cup USA (total 34 nationally), 2014
14. PandaCare, Honorable Mention of Cornell Cup USA (total 10 nationally), 2013
15. Beiye Liu, A. Richard Newton Young Fellow Program ($675) for DAC 2013.
16. Kent W. Nixon, A. Richard Newton Young Fellow Program ($575) for DAC 2013.

17. **Wujie Wen, 49th Design Automation Conference A. Richard Newton Scholarship ($24,000), 2012.**
18. Wujie Wen, Youth Student Support Program (YSSP, $610) for DAC 2012.
19. Xiang Chen, Youth Student Support Program (YSSP, $610) for DAC 2012.
20. Wujie Wen, Travel grant ($500) for ACM Student Research Competition at DAC 2012.
21. Xiang Chen, Travel grant ($500) for ACM Student Research Competition at DAC 2012.
22. Kent W. Nixon, Air Force Visiting Student Scholarship, AFRL/RIB, Rome, NY, 2012 summer.
23. Peiyuan Wang, Graduate travel grant ($350) for Non-Volatile Memories Workshop, 2012.
24. Wujie Wen, Graduate travel grant ($350) for Non-Volatile Memories Workshop, 2012.
25. Xiang Chen, Graduate travel grant ($350) for Non-Volatile Memories Workshop, 2012.
26. Jie Guo, Graduate travel grant ($350) for Non-Volatile Memories Workshop, 2012.
27. Peiyuan Wang, IEEE Magnetics Society Student Travel Grant ($1000) for IEEE International Magnetics Conference, 2011.
28. Yaojun Zhang, Graduate travel grant ($300) for Non-Volatile Memories Workshop, 2011.

REFERENCES

1. **Leon Chua**, Ph.D.
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