

Hai (Helen) Li

Evolutionary Intelligence Laboratory (<http://ei-lab.org>)

Department of Electrical & Computer Engineering
Swanson School of Engineering
University of Pittsburgh
Pittsburgh, PA 15261

Phone: +1 (412) 648-9597
Fax: +1 (412) 624-8003
Email: hal66@pitt.edu
hai.helen.li@gmail.com

A. RESEARCH INTEREST

Traditional and Emerging Memory Design and Architecture
Brain-Inspired Computing Systems, Neuromorphic Design
Device/Circuit/Architecture Co-optimization for Low Power & High Performance

B. EDUCATION

- Ph.D.** in Electrical and Computer Engineering, Purdue University, August 2004.
Thesis: Low-Power Design Technique at Circuit and Microarchitectural Levels
Advisor: Professor Kaushik Roy
- M.S.** in Microelectronics, Tsinghua University, July 2000.
Thesis: BSIM3V3 Model Parameter Extraction and Its Application in Technology
Advisor: Professor Jimin Wang
- B.S.*** in Electronic Engineering, Tsinghua University, June 1998.
Thesis: Deep Sub-micron Device Manufacture with Emphasis on Oxide Spacer Manufacture
Advisor: Professor Teng'ge Ma
** Graduated within 4 years under a 5-year undergraduate program*

C. PROFESSIONAL EXPERIENCE

- Assistant Professor** *September 2012–present*
Dept. of Electrical and Computer Engineering, Swanson School of Engineering, University of Pittsburgh
- Assistant Professor** *September 2009–August 2012*
Dept. of Electrical and Computer Engineering, Polytechnic Institute of New York University
- Senior Staff Engineer** *April 2007–July 2009*
Memory Product Group, Seagate Technology LLC, Bloomington, MN.
- Senior Design Engineer** *December 2005–April 2007*
Microprocessor Product Group, Intel Corporation, Santa Clara, CA.
- Senior Design Engineer** *September 2004–December 2005*
Qualcomm CDMA Technology, Qualcomm Inc., San Diego, CA.

D. HONORS AND AWARDS

- 1) **DARPA Young Faculty Award (YFA)**, 2013.
- 2) **NSF Career Program**, 2012.
- 3) **Air Force Visiting Faculty Research Program (VFRP) Fellowship**, AFRL/RIB, Rome, NY, 2013.
- 4) WICAT Center and NYU WIRELESS Research Distribution Award, 2012.
- 5) **Air Force Summer Faculty Fellowship Program Award (AF-SFFP)**, AFRL/RITC, Rome, NY, 2011.
(*Ranking 2 of 300+ applicants*)
- 6) **Best Paper Award**, *Asia and South Pacific Design Automation Conference (ASPDAC)* for the paper titled “Quantitative Modeling of Racetrack Memory – A Tradeoff among Area, Performance, and Power,” 2015.
- 7) **Best Paper Award**, *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)* for the paper titled “A Weighted Sensing Scheme for ReRAM-based Cross-point Memory Array,” 2014.
- 8) **Best Paper Award**, *Proceedings of the 23rd ACM International Conference on Great Lakes Symposium on VLSI (GLSVLSI)* for the paper titled “Coordinating Prefetching and STT-RAM based Last-level Cache

Management for Multicore Systems,” 2013.

- 9) **Best Paper Award**, *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)* for the paper titled “Combined Magnetic- and Circuit-level Enhancements for the Nondestructive Self-Reference Scheme of STT-RAM,” 2010.
- 10) **Best Paper Award**, *the 9th International Symposium on Quality Electronic Design (ISQED)* for paper titled “Design Margin Exploration of Spin-Torque Transfer RAM (SPRAM),” 2008.
- 11) **Best Paper Nomination**, *International Conference on Computer Aided Design (ICCAD)* for the paper titled “Unleashing the Potential of MLC STT-RAM Caches,” 2013.
- 12) **Best Paper Nomination**, *International Conference on Computer Aided Design (ICCAD)* for the paper titled “Probabilistic Design Methodology to Improve Run-time Stability and Performance of STT-RAM Caches,” 2012.
- 13) **Best Paper Nomination**, *Asia and South Pacific Design Automation Conference (ASP-DAC)* for the paper titled “Geometry Variations Analysis of TiO₂ Thin Film and Spintronic Memristors,” 2011.
- 14) **Best Paper Nomination**, *Design, Automation & Test in Europe Conference and Exhibition (DATE)* for the paper titled “A Nondestructive Self-Reference Scheme for Spin-Transfer Torque Random Access Memory (STT-RAM),” 2010.
- 15) **Best Paper Nomination**, *the 11th International Symposium on Quality Electronic Design (ISQED)* for the paper titled “Scalability of PCMO-based Resistive Switch Device in DSM Technologies,” 2010.

E. RESEARCH GRANTS

Federal Funding (Total personal allocation: \$2,239,171)

- 1) *Air Force Research Lab (AFRL), FA8750-15-2-0048*: Hai Li (PI, 50%), Yiran Chen (co-PI, 50%), “The Design of Neuromorphic Controller System Built with Memristor Crossbars,” 01/01/2015-09/30/2017, \$750,000.
- 2) *Air Force Research Lab (AFRL), FA8750-14-1-0241*: Hai Li (PI, 50%), Yiran Chen (co-PI, 50%), “Neuromorphic Computing Engine with Resistive Crossbar Architecture,” 09/19/2014-02/18/2015, \$118,047.
- 3) *National Science Foundation (NSF), CCF-1337198*: Qinru Qiu (Lead-PI, Syracuse, 38%), Hai Li (PI, Pitt, 31%), Yiran Chen (co-PI, Pitt, 31%), “NeoNexus: The Next-generation Information Processing System across Digital and Neuromorphic Computing Domains,” 09/2013–06/2017, \$725,884.
- 4) *Defense Advanced Research Projects Agency (DARPA) Young Faculty Award (YFA), D13AP00042*: Hai Li (PI, 100%), “An Adaptive Information Processing System Resilient to Device Variations and Noises,” 08/2013–07/2015, \$500,000.
- 5) *Air Force Research Lab (AFRL), FA8750-13-2-0115*: Yiran Chen (PI, 50%), Hai Li (co-PI, 50%), “Memristor Crossbar Based Computing Engine for High Performance and Power Efficiency,” 08/01/2013-10/31/2013, \$50,000.
- 6) *National Science Foundation (NSF), CNS-1311706 (prev. CNS-1149654)*: Hai Li (PI, 100%), “CAREER: STT-RAM based Memory Hierarchy and Management in Embedded Systems,” 09/2012–08/2017, \$450,000.
- 7) *National Science Foundation (NSF), EECS-1311747 (prev. ECCS-1202236)*: Hai Li (Lead-PI, 50%), Yiran Chen (PI, 50%), “SMURFS: Statistical Modeling, SimUlation and Robust Design Techniques For Memristors,” 5/1/2012–4/30/2015, \$500,149.
- 8) *National Science Foundation (NSF), CNS-1342566 (prev. CNS-1116684)*: Hai Li (Lead-PI, 50%), Yiran Chen (PI, 50%), “Cross-Layer Design Techniques for Robustness of the Next-generation Nonvolatile Memories,” 09/2011–08/2014, \$450,000.
- 9) *Air Force Research Lab (AFRL), FA8750-11-2-0046*: Hai Li (PI, 100%), “Memristor-Based Computing Architecture: Design Methodologies & Circuit Techniques,” 10/2010–10/2012, \$130,000.

Industry Funding (Total personal allocation: \$70,000)

- 10) *Cisco Systems Inc.*: Hai Li (PI, 100%), Gifted Research Grant, 2014, \$50,000.
- 11) *Qualcomm Inc.*: Hai Li (PI, 50%), Yiran Chen (co-PI, Pitt, 50%), Gifted Research Grant, 2014, \$40,000.

Internal Funding (Total personal allocation: \$310,000)

- 12) Hai Li (PI), WICAT Center and NYU WIRELESS Research Distribution Award, \$10,000, 2012.

- 13) Hai Li (PI), Jonathan Chao, and Yuan Xie, “Workshop on 3D Integration for Future High Performance Computer Architecture,” NYU-ADI, \$300,000. (Workshop was held on April 18-19, 2011 at Abu Dhabi)

International Collaborations (Note: the program policy restricts the funding usage outside the country)

- 14) *National Program on Key Basic Research Project (973 Program), China, 2010CB934400*: Hai Li (Senior Personnel 0%, PI: Hanming Wu), “Physical Study and Development on Nano-magnetic Spintronic Memory and Semiconductor Silicon-based Quantum Dot Memory,” 01/2010–08/2014, \$3.14M.
- 15) *National Program on Major Research Instrumentation Development, China, 2011YQ120053*: Hai Li (Senior Personnel 0%, PI: Xiufeng Han), “Virtualization of Nanotechnology and The Measurement System of Ultra-Spectrum Electro-magnetic Property,” 01/2011–09/2015, \$9.37M.

F. LIST OF PUBLICATIONS

(i) Books

- B1. H. Li and Y. Chen, *Nonvolatile Memory Design: Magnetic, Resistive, and Phase Changing*, CRC Press, December 2011, ISBN: 978-14-398-0745-3. ([Amazon link](#))

(ii) Book Chapters

- Bc7. H. Li and M. Hu, “Modeling of Memristor at nanoscale – Static, Statistical, and Stochastic Methodologies,” a book chapter in *CMOS and Post-CMOS Perspectives of Electronic Device Scaling*, edited by Saraju Mohanty, Springer, 2015, to appear.
- Bc6. Y. Zhang, W. Wen, H. Li, and Y. Chen “*The Prospect of STT-RAM Scaling*,” a book chapter in *Metallic Spintronic Devices*, edited by Xiaobin Wang, CRC Press, 2014, ISBN 978-1-4665-8844-8. ([CRC link](#))
- Bc5. Y. Chen, H. Li, and *Z. Sun, “*Spintronic Memristor as Interface between DNA and Solid State Devices*,” a book chapter in *Memristors and Memristive Systems*, edited by Ronald Tetzlaff, Springer, 2014, ISBN: 978-1-4614-9067-8. ([Springer link](#))
- Bc4. H. Li, Z. Sun, X. Bi, W.-F. Wong, X. Zhu, and W. Wu, “*STT-RAM Cache Hierarchy Design and Exploration with Emerging Magnetic Devices*,” a book chapter in *Emerging Memory Technologies – Design, Architecture, and Applicants*, edited by Yuan Xie, Springer, 2014, ISBN: 978-1-4419-9550-6. ([Springer link](#))
- Bc3. H. Li and R. E. Pino, “*Statistical Memristor Model and Its Applications in Neuromorphic Computing*,” a book chapter in *Advances in Neuromorphic Memristor Science and Applications*, edited by R. Kozma, R. E. Pino, and G. Puzanica, Springer, 2012, ISBN 978-94-007-4490-5. ([Springer link](#))
- Bc2. Y. Chen, H. Li, Y. Xie, and D. Niu, “*Low Power Design of Emerging Memory Technologies*,” a book chapter in *Handbook of Energy-Aware and Green Computing*, edited by Ishfaq Ahmad and Sanjay Ranka, CRC Press, 2012, ISBN: 978-14-398-5040-4. ([Amazon link](#))
- Bc1. H. Li, R. Patel, K. Sit, Z. Tang and S. Jamshidi, “*Design for Low Power*,” a book chapter in *The Computer Engineering Handbook*, the second edition, edited by V. Oklobdzija, CRC Press, 2008, ISBN 978-08-493-0885-7. ([Amazon link](#))

(iii) Refereed Journal Articles

- J36. S. Duan, Z. Dong, X. Hu, L. Wang, and H. Li, “Small-world Hopfield neural networks with weight salience priority and memristor synapses for digit recognition,” *Neural Computing and Applications*, Volume 2015, April 2015. (DOI: 10.1007/s00521-015-1899-7)
- J35. Z. Sun, X. Bi, W. Wu, S. Yoo, and H. Li, “Array Organization and Data Management Exploration in Race-track Memory,” to appear in *IEEE Transactions on Computers (TC)*. (DOI: 10.1109/TC.2014.2360545)
- J34. Y. Zhang, Y. Li, Z. Sun, H. Li, Y. Chen, and Alex K. Jones, “Read Performance: The Newest Barrier in Scaled STT-RAM,” to appear in *IEEE Transactions on Very Large Scale Integration (TVLSI) Systems*. (DOI: 10.1109/TVLSI.2014.2326797)
- J33. E. Eken, Y. Zhang, W. Wen, R. Joshi, H. Li, and Y. Chen, “A Novel Self-reference Technique for STT-RAM Read and Write Reliability Enhancement,” *IEEE Transaction on Magnetics (TMAG)*, vol. 50, no. 11, article 3401404, Nov. 2014. (DOI: 10.1109/TMAG.2014.2323196)
- J32. M. Hu, H. Li, Y. Chen, Q. Wu, G. Rose, and W. Linderman, “Memristor Crossbar Based Neuromorphic Computing System: A Case Study,” *IEEE Transactions on Neural Network and Learning System (TNNLS)*, vol. 25, no 10, pp. 1864-1878, Oct. 2014. (DOI: 10.1109/TNNLS.2013.2296777)
- J31. Z. Dong, S. Duan, X. Hu, L. Wang, and H. Li, “A Novel Memristive Multilayer Feedforward Small-World

- Neural Network with its Applications in PID Control,” *the Scientific World Journal*, Volume 2014, Article ID 394828, August 2014. (DOI: 10.1155/2014/394828)
- J30. Z. Sun, X. Bi, H. Li, W.-F. Wong, and X. Zhu, “STT-RAM Cache Hierarchy with Multi-retention MTJ Designs,” *IEEE Transactions on Very Large Scale Integration (TVLSI) Systems*, volume 22, issue 6, June 2014, pages 1281-1293. (DOI: 10.1109/TVLSI.2013.2267754)
- J29. Y. Li, Y. Zhang, H. Li, Y. Chen, and A. Jones, “C1C: A Configurable, Compiler-guided STT-RAM L1 Cache,” *European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC) also ACM Transactions on Architecture and Code Optimization (TACO)*, volume 110, issue 4, Dec. 2013, article no. 52. (DOI: 10.1145/2541228.2555308)
- J28. B. Zhao, J. Yang, Y. Zhang, Y. Chen, and H. Li, “Architecting a Common-Source-Line Array for Bipolar Non-Volatile Memory Devices,” *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, volume 8, issue 4, Oct. 2013, article no 57. (DOI: 10.1145/2500459)
- J27. Y. Chen, W.-F. Wong, H. Li, C.-K. Cheng, Y. Zhang, and W. Wen, “On-chip Caches Built on Multi-level Spin-transfer Torque RAM Cells and Its Optimizations,” *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, volume 9, issue 2, May 2013, article no. 16. (DOI: 10.1145/2463585.2463592)
- J26. Z. Sun, H. Li, Y. Chen, and X. Wang, “Voltage Driven Non-Destructive Self-Reference Sensing Scheme of Spin-Transfer Torque Memory,” *IEEE Transactions on Very Large Scale Integration (TVLSI) Systems*, volume 20, issue 11, November 2012, pages 2020-2030. (DOI: 10.1109/TVLSI.2011.2166282)
- J25. X. Bi, H. Li, and X. Wang, “STT-RAM Cell Design Considering CMOS and MTJ Temperature Dependence,” *IEEE Transaction on Magnetics (TMAG)*, volume 48, issue 11, November 2012, pages 3821-3824. (DOI: 10.1109/TMAG.2012.2200469)
- J24. Y.-C. Chen, H. Li, W. Zhang and R. Pino, “The 3D Stacking Bipolar RRAM for High Density,” *IEEE Transaction on Nanotechnology (TNANO)*, volume 11, issue 5, September 2012, pages 948-956. (DOI: 10.1109/TNANO.2012.2208759)
- J23. H. Li and Z. Sun, “Voltage Driven Non-destructive Self-reference Sensing for STT-RAM Yield Enhancement,” *Spin*, volume 2, issue 3, September 2012, pages 124008. (DOI: 10.1142/S2010324712400085)
- J22. Z. Sun, X. Chen, Y. Zhang, H. Li, and Y. Chen, “Nonvolatile Memories as the Data Storage System for Implantable ECG Recorder,” *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, volume 8, issue 2, , June 2012, article no. 13. (DOI: 10.1145/2180878.2180885)
- J21. Z. Sun, H. Li, X. Wang, and Y. Chen, “MTJ Design Margin Exploration for Self-Reference Sensing,” *Journal of Applied Physics (JAP)*, volume 111, March 2012, pages 07C726. (DOI: 10.1063/1.3679647)
- J20. Y. Chen, H. Li, X. Wang, W. Zhu, W. Xu and T. Zhang, “A 130 nm 1.2V/3.3V 16 Kb Spin-Transfer Torque Random Access Memory with Nondestructive Self-Reference Sensing Scheme,” *IEEE Journal of Solid-State Circuits (JSSC)*, volume 47, issue 2, February 2012, pages 560-573. (DOI: 10.1109/JSSC.2011.2170778)
- J19. H. Li, X. Wang, Z.-L. Ong, W.-F. Wong, Y. Zhang, P. Wang and Y. Chen, “Performance, Power and Reliability Tradeoffs of STT-RAM Cell Subjective to Architecture-level Requirement,” *IEEE Transaction on Magnetics (TMAG)*, volume 47, issue 10, October 2011, pages 2356-2359. (COI: 10.1109/TMAG.2011.2159262)
- J18. Y. Zhang, X. Wang, H. Li, and Y. Chen, “STT-RAM Cell Optimization Considering Process Variations,” *IEEE Transaction on Magnetics (TMAG)*, volume 47, issue 10, October 2011, pages 2962-2965. (DOI: 10.1109/TMAG.2011.2158810)
- J17. P. Wang, X. Wang, Y. Zhang, H. Li and Y. Chen, “Nonpersistent Errors Optimization in Spin-MOS Logic and Storage Circuitry,” *IEEE Transaction on Magnetics (TMAG)*, volume 47, issue 10, October 2011, pages 3860-3863. (DOI: 10.1109/TMAG.2011.2153838)
- J16. X. Dong, X. Wu, Y. Xie, Y. Chen, and H. Li, “Stacking MRAM atop Microprocessors: An Architecture-Level Evaluation,” *IET Computers & Digital Techniques (IET-CDT)*, volume 5, issue 3, June 2011, pages 213-220. (DOI: 10.1049/iet-cdt.2009.0091)
- J15. M. Hu, H. Li, Y. Chen, and X. Wang, “Spintronic Memristor: Compact Model and Statistical Analysis,” *Journal of Low Power Electronics (JOLPE)*, volume 7, number 2, April 2011, pages 234-244. (DOI: 10.1166/jolpe.2011.1131)
- J14. W. Zhu, H. Li, Y. Chen, and X. Wang, “Current Switching in MgO-based Magnetic Tunneling Junctions,” *IEEE Transaction on Magnetics (TMAG)*, volume 47, issue 1, part 2, January 2011, pages 156-160. (DOI: 10.1109/TMAG.2010.2085441)

- J13. Y. Chen, X. Wang, H. Li, H. Xi, W. Zhu and Y. Yan, "Design Margin Exploration of Spin-Transfer Torque RAM (STT-RAM) in Scaled Technologies", *IEEE Transactions on Very Large Scale Integration (TVLSI) Systems*, volume 18, issue 12, December 2010, pages 1724-1734. (DOI: 10.1109/TVLSI.2009.2032192)
- J12. Y. Chen, H. Li, C.-K. Chen, K. Roy, J. Li and G. Sun, "Variable-Latency Adder (VL-Adder) Designs for Low Power and NBTI Tolerance", *IEEE Transactions on Very Large Scale Integration (TVLSI) Systems*, volume 18, issue 11, October 2010, pages 1621-1624. (DOI: 10.1109/TVLSI.2009.2026280)
- J11. Y. Chen, W. Tian, H. Li, X. Wang, W. Zhu, "PCMO Device with High Switching Stability," *IEEE Electron Device Letters (EDL)*, volume 31, issue 8, August 2010, pages 866-868. (DOI: 10.1109/LED.2010.2050457)
- J10. H. Xi, J. Stricklin, H. Li, Y. Chen, X. Wang, Y. Zheng, Z. Gao, and M. X. Tang, "Spin Transfer Torque Memory with Thermal Assist Mechanism: A Case Study," *IEEE Transaction on Magnetics (TMAG)*, volume 46, issue 3, March 2010, pages 860-865. (DOI: 10.1109/TMAG.2009.2033674)
- J9. X. Wang, Y. Chen, Y. Gu, and H. Li, "Spintronic Memristor Temperature Sensor," *IEEE Electron Device Letters (EDL)*, volume 31, issue 1, January 2010, pages 20-22. (DOI: 10.1109/LED.2009.2035643)
- J8. Y. Chen, H. Li, C.-K. Chen and K. Roy, "Gated Decap: Gate Leakage Control of On-chip Decoupling Capacitors in Scaled Technologies", *IEEE Transactions on Very Large Scale Integration (TVLSI) Systems*, volume 17, issue 12, December 2009, pages 1749-1752. (DOI: 10.1109/TVLSI.2008.2007843)
- J7. C.-K. Koh, W.-F. Wong, Y. Chen and H. Li, "Tolerating process variations in large, set associative caches: The buddy cache", *ACM Transactions on Architecture and Code Optimization (TACO)*, volume 6, issue 2, article no. 8, June 2009 (**34 pages**). (DOI: 10.1145/1543753.1543757)
- J6. X. Wang, H. Xi, Y. Chen, H. Li and D. V. Dimitrov, "Spintronic Memristor through Spin Torque Induced Magnetization Motion", *IEEE Electron Device Letters (EDL)*, volume 30, issue 3, March 2009, pages 294-297. (**Interviewed by IEEE Spectrum**) (DOI: 10.1109/LED.2008.2012270)
- J5. X. Wang, Y. Chen, H. Li, H. Liu and D. Dimitrov, "Spin Torque Random Access Memory down to 22nm Technology", *IEEE Transaction on Magnetics (TMAG)*, volume 44, issue 11, November 2008, pages 2479-2482. (DOI: 10.1109/TMAG.2008.2002386)
- J4. H. Li, C.-Y. Cher, T. N. Vijaykumar, and K. Roy, "Combined Circuit and Architectural Level Variable Supply-Voltage Scaling for Low Power", *IEEE Transaction on Very Large Scale Integration (TVLSI) Systems*, volume 13, issue 5, May 2005, pages 564-576. (DOI: 10.1109/TVLSI.2005.844295)
- J3. H. Li, S. Bhunia, Y. Chen, T. N. Vijaykumar, and K. Roy, "DCG: Deterministic Clock Gating For Low-Power Microprocessor Design," *IEEE Transactions on Very Large Scale Integration (TVLSI) Systems*, volume 12, issue 3, March 2004, pages 245-254. (DOI: 10.1109/TVLSI.2004.824307)
- J2. Agarwal, H. Li, and K. Roy, "A Single- V_t Low-Leakage Gated-Ground Cache for Deep Submicron", *IEEE Journal of Solid-State Circuits (JSSC)*, volume 38, issue 2, February 2003, pages 319-328. (DOI: 10.1109/JSSC.2002.807414)
- J1. H. Li, J. Wang, Z. Liu, and H. Qing, "An Optimal Strategy for Parameter Extraction of BSIM3V3 Model", *Microelectronics (微电子学 in Chinese)*, volume 30, issue 6, 2000, pages 387-390. (Link)

(iv) Peer Reviewed Conference Publications

- C74. J. Guo, J. Hu, D. Wang, H. Li, and Y. Chen, "FlexLevel: a Novel NAND Flash Storage System Design for LDPC Latency Reduction," *Proceedings of the 51st Annual Design Automation Conference (DAC)*, June 2015.
- C73. B. Liu, X. Li, Q. Wu, T. Huang, H. Li, and Y. Chen, "Vortex: Variation-aware Training for Memristor X-bar," *Proceedings of the 51st Annual Design Automation Conference (DAC)*, June 2015.
- C72. M. Mao, J. Hu, H. Li, and Y. Chen, "VWS: A Versatile Warp Scheduler for Exploring Diverse Cache Localities of GPGPU Applications," *Proceedings of the 51st Annual Design Automation Conference (DAC)*, June 2015.
- C71. X. Liu, M. Mao, et al. "Harmonica: A Heterogeneous Architecture with Hierarchical Neuromorphic Computing Accelerator Design" *Proceedings of the 51st Annual Design Automation Conference (DAC)*, June 2015.
- C70. C. Liu, B. Yan, C. Yang, L. Song, Z. Li, B. Liu, Q. Wu, H. Jiang, Y. Chen, and H. Li, "A Spiking Neuromorphic Design with Memristor Crossbar," *Proceedings of the 51st Annual Design Automation Conference (DAC)*, June 2015.

- C69. Z. Li, B. Yan, L. Yang, W. Zhao, Y. Chen, and H. Li, "A New Self-reference Sensing Scheme for TLC MRAM," *IEEE International Symposium on Circuits and Systems (ISCAS)*, June 2015.
- C68. S. Li, C. Wu, B. Li, Y. Wang, Q. Qiu, and H. Li, "FPGA Acceleration of Recurrent Neural Network based Language Model," *the 23rd IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, May 2015.
- C67. B. Yan, Z. Li, Y. Zhang, J. Yang, W. Zhao, P. C.-F. Chia, and H. Li, "A High-Speed Robust NVM-TCAM Design Using Body Bias Feedback," *Proceedings of the 25th ACM International Conference on Great Lakes Symposium on VLSI (GLSVLSI)*, May 2015.
- C66. Y. Wang, W. Wen, M. Hu, and H. Li, "A Novel True Random Number Generator Design Leveraging Emerging Memristor Technology," *Proceedings of the 25th ACM International Conference on Great Lakes Symposium on VLSI (GLSVLSI)*, May 2015.
- C65. C. Zhang, G. Sun, W. Zhang, F. Mi, H. Li, and W. Zhao, "Quantitative Modeling of Racetrack Memory, A Tradeoff among Area, Performance, and Power," *the 19th Asia and South Pacific Design Automation Conference (ASPDAC)*, January 2015, pages 100-105. **(Best Paper Award)** (DOI: 10.1109/ASPDAC.2015.7058988)
- C64. X. Liu, M. Mao, X. Bi, H. Li, and Y. Chen, "STT-RAM based Register File in GPU Architectures," *the 19th Asia and South Pacific Design Automation Conference (ASPDAC)*, January 2015, pages 490-495. (DOI: 10.1109/ASPDAC.2015.7059054)
- C63. B. Liu, H. Li, Y. Chen, X. Li, T. Huang, Q. Wu, and M. Barnell, "Reduction and IR-drop Compensation Techniques for Reliable Neuromorphic Computing," *International Conference on Computer Aided Design (ICCAD)*, November 2014, pages 63-70. (DOI: 10.1109/ICCAD.2014.7001330)
- C62. J. Wang, W.-F. Wong, and H. Li, "Optimizing MLC-based STT-RAM Caches by Dynamic Block Size Reconfiguration," *the 32nd IEEE International Conference on Computer Design (ICCD)*, October 2014. (DOI: 10.1109/ICCD.2014.6974672)
- C61. X. Liu, M. Mao, H. Li, Y. Chen, H. Jiang, J. Yang, Q. Wu, and M. Barnell, "A Heterogeneous Computing System with Memristor-Based Neuromorphic Accelerators," *IEEE High Performance Extreme Computing Conference (HPEC)*, September 2014, pages 1-6. (DOI: 10.1109/HPEC.2014.7040986)
- C60. Z. Sun, X. Bi, A. K. Jones, and H. Li, "Design Exploration of Racetrack Lower-level Caches," in *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, August 2014. (DOI: 10.1145/2627369.2627651)
- C59. C. Liu, and H. Li, "A Weighted Sensing Scheme for ReRAM-based Cross-point Memory Array," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2014. **(Best Paper Award)** (DOI: 10.1109/ISVLSI.2014.32)
- C58. X. Hu, G.-F., H. Li, Y. Chen, and S. Duan, "An Adjustable Memristor Model and Its Application in Small-world Neural Networks," *International Joint Conference on Neural Networks (IJCNN)*, July 2014, pages 7-14. (DOI: 10.1109/IJCNN.2014.6889605)
- C57. L. Chen, C. Li, T. Huang, X. He, H. Li, and Y. Chen, "STDP Learning Rule Based on Memristor with STDP Property," *International Joint Conference on Neural Networks (IJCNN)*, July 2014, pages 1-6. (DOI: 10.1109/IJCNN.2014.6889506)
- C56. E. Eken, Y. Zhang, W. Wen, R. Joshi, H. Li, and Y. Chen, "A New Field-assisted Access Scheme of STT-RAM with Self-reference Capability," *Proceedings of the 50th Annual Design Automation Conference (DAC)*, June 2014, pages 1-6. (DOI: 10.1145/2593069.2593075)
- C55. M. Mao, W. Wen, Y. Zhang, H. Li, and Y. Chen, "Exploration of GPGPU Register File Architecture Using Domain-wall-shift-write based Racetrack Memory," *Proceedings of the 50th Annual Design Automation Conference (DAC)*, June 2014, pages 1-6. (DOI: 10.1145/2593069.2593137)
- C54. E. Park, S. Yoo, S. Lee, and H. Li, "Accelerating Graph Computation with Racetrack Memory and Pointer-Assisted Graph Representation," *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, March 2014, pages 1-4. (DOI: 10.7873/DATE2014.172)
- C53. B. Li, Y. Wang, Y. Chen, H. Li, and H. Yang, "ICE: Inline Calibration for Memristor Crossbar-based Computing Engine," *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, March 2014, pages 1-4. (DOI: 10.7873/DATE2014.197)
- C52. J. Wang, Y. Tim, W.-F. Wong, Z.-L. Ong, Z. Sun, and H. Li, "A Coherent Hybrid SRAM and STT-RAM L1 Cache Architecture for Shared Memory Multicores," *the 19th Asia and South Pacific Design Automation Conference (ASPDAC)*, January 2014, pages 610-615. (DOI: 10.1109/ASPDAC.2014.6742958)

- C51. M. Hu, Y. Wang, Q. Qiu, Y. Chen, and H. Li, "The Stochastic Modeling of TiO₂ Memristor and Its Usage in Neuromorphic System Design," in *the 19th Asia and South Pacific Design Automation Conference (ASPDAC)*, January 2014, pages 831-836. (DOI: 10.1109/ASPDAC.2014.6742993)
- C50. Y. Zhang, I. Bayram, Y. Wang, H. Li, and Y. Chen, "ADAMS: Asymmetric Differential STT-RAM Cell Structure For Reliable and High-performance Applications," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2013, pages 9-16. (DOI: 10.1109/ICCAD.2013.6691091)
- C49. X. Bi, M. Mao, D. Wang, and H. Li, "Unleashing the Potential of MLC STT-RAM Caches," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2013, pages 429-436. (**Best Paper Nomination**) (DOI: 10.1109/ICCAD.2013.6691153)
- C48. J. Wang, Z. Sun, H. Li, and W.-F. Wong, "Practical Low-Power Memristor-based Analog Neural Branch Predictor," *International Symposium on Low Power Electronics and Design (ISLPED)*, September 2013, pages 175-180. (DOI: 10.1109/ISLPED.2013.6629290)
- C47. Y.-C. Chen, W. Zhang, and H. Li, "A Hardware Security Scheme for RRAM-based FPGA," *the 23rd International Conference on Field Programmable Logic and Applications (FPL)*, August 2013, pages 1-4. (DOI: 10.1109/FPL.2013.6645556)
- C46. F. Ji, H. Li, B. Wysocki, C. Thiem, and N. McDonald "Memristor-based Synapse Design and a Case Study in Reconfigurable Systems," *International Joint Conference on Neural Networks (IJCNN)*, August 2013, article no. 1029. (DOI: 10.1109/IJCNN.2013.6706776)
- C45. B. Liu, M. Hu, H. Li, Z.-H. Mao, Y. Chen, T. Huang, and W. Zhang, "Digital-Assisted Noise Eliminating Training For Memristor Crossbar-Based Analog Neuromorphic Computing Engine," *Proceedings of the 50th Annual Design Automation Conference (DAC)*, June 2013, Article no. 7. (DOI: 10.1145/2463209.2488741)
- C44. Z. Sun, W. Wu, and H. Li, "Cross-Layer Racetrack Memory Design For Ultra High Density And Low Power Consumption," *Proceedings of the 50th Annual Design Automation Conference (DAC)*, June 2013, Article no. 53. (DOI: 10.1145/2463209.2488799)
- C43. M. Mao, H. Li, A. Jones, and Y. Chen, "Coordinating Prefetching and STT-RAM based Last-level Cache Management for Multicore Systems," *Proceedings of the 23rd ACM International Conference on Great Lakes Symposium on VLSI (GLSVLSI)*, May 2013, pages 55-60. (**Best Paper Award, 1 out of 20 in track, 5.0%**) (DOI: 10.1145/2483028.2483060)
- C42. M. Hu, H. Li, Y. Chen, Q. Wu, and G. Rose, "BSB Training Scheme Implementation on Memristor-Based Circuit," *2013 IEEE Symposium on Computational Intelligence for Security and Defense Applications (CISDA)*, April 2013, pages 80-87. (DOI: 10.1109/CISDA.2013.6595431)
- C41. J. Guo, W. Wen, Y. Zhang, H. Li and Y. Chen, "DA-RAID-5: A Disturb Aware Data Protection Technique for NAND Flash Storage Systems," *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, March 2013, pages 380-385. (DOI: 10.7873/DATE.2013.087)
- C40. X. Bi, A. M. Weldon, and H. Li, "STT-RAM Designs Supporting Dual-port Accesses," *Design, Automation & Test in Europe Conference and Exhibition (DATE)*, March 2013, pages 853-858. (DOI: 10.7873/DATE.2013.180)
- C39. Y.-C. Chen, W. Wang, W. Zhang, and H. Li, "uBRAM-based Run-time Reconfigurable FPGA and Corresponding Reconfiguration Methodology," *International Conference on Field-Programmable Technology (FPT)*, December 2012, pages 80-86. (DOI: 10.1109/FPT.2012.6412116)
- C38. X. Bi, Z. Sun, H. Li, and W. Wu, "Probabilistic Design Methodology to Improve Run-time Stability and Performance of STT-RAM Caches," *International Conference on Computer Aided Design (ICCAD)*, November 2012, pp. 88-94. (**Best Paper Nomination**) (DOI: 10.1145/2429384.2429401)
- C37. Y.-C. Chen, W. Zhang, and H. Li, "Non-volatile 3D stacking RRAM-based FPGA," *the 22nd International Conference on Field Programmable Logic and Applications (FPL)*, August 2012, pages 367-372. (DOI: 10.1109/FPL.2012.6339206)
- C36. Z. Sun, H. Li, and W. Wu, "A Dual-mode Architecture for Fast-switching STT-RAM," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, August 2012, pages 45-50. (DOI: 10.1145/2333660.2333673)
- C35. Z. Sun, X. Bi, and H. Li, "Process Variation Aware Data Management for STT-RAM Cache Design," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, August 2012, pages 179-184. (DOI: 10.1145/2333660.2333706)

- C34. M. Hu, H. Li, Q. Wu, G. Rose, and Y. Chen, "Memristor Crossbar Based Hardware Realization of BSB Recall Function," *International Joint Conference on Neural Networks (IJCNN)*, June 2012, pages 1-7. (DOI: 10.1109/IJCNN.2012.6252563)
- C33. H. Wang, H. Li, and R. E. Pino, "Memristor-based Synapse Design and Training Scheme for Neuromorphic Computing Architecture," *International Joint Conference on Neural Networks (IJCNN)*, June 2012, pages 1-5. (DOI: 10.1109/IJCNN.2012.6252577)
- C32. M. Hu, H. Li, Q. Wu, and G. Rose, "Hardware Realization of Neuromorphic BSB Model with Memristor Crossbar Network," *Proceedings of the 49th Annual Design Automation Conference (DAC)*, June 2012, pages 498-503. (DOI: 10.1145/2228360.2228448)
- C31. Y.-C. Chen, H. Li, and W. Zhang, "A Novel Peripheral Circuit for RRAM-based LUT," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Korean, May 2012, pages 1811-1814. (DOI: 10.1109/ISCAS.2012.6271619)
- C30. X. Bi, C. Zhang, H. Li, Y. Chen, and R. Pino, "Spintronic Memristor Based Temperature Sensor Design with CMOS Current Reference," *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Dresden, Germany, March 2012, pages 1301-1306. (DOI: 10.1109/DATE.2012.6176693)
- C29. B. Zhao, J. Yang, Y. Zhang, Y. Chen and H. Li, "Architecting a Common-source-line Array for Bipolar Nonvolatile Memory Devices," *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Germany, March 2012, pages 1451-1454. (DOI: 10.1109/DATE.2012.6176594)
- C28. Y.-C. Chen, W. Zhang, and H. Li, "A Look Up Table Design with 3D Bipolar RRAMs," *the 17th Asia and South Pacific Design Automation Conference (ASPDAC)*, January 2012, pages 73-78. (DOI: 10.1109/ASPDAC.2012.6165051)
- C27. X. Chen, J. Zeng, Y. Chen, W. Zhang, and H. Li, "Fine-grained Dynamic Voltage Scaling on OLED Display," *the 17th Asia and South Pacific Design Automation Conference (ASPDAC)*, January 2012, pages 807-812. (DOI: 10.1109/ASPDAC.2012.6165066)
- C26. Z. Sun, X. Bi, H. Li, W.-F. Wong, Z.-L. Ong, X. Zhu and W. Wu, "Multi Retention Level STT-RAM Cache Designs," *Proceedings of the 44th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2011, pages 329-338. (DOI: 10.1145/2155620.2155659)
- C25. M. Hu, H. Li, and R. E. Pino, "Fast Statistical Model of TiO₂ Memristor and Design Implication," *IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, November 2011, pages 345-352. (DOI: 10.1109/ICCAD.2011.6105353)
- C24. P. Wang, X. Chen, Y. Chen, H. Li, S. Kang, X. Zhu, W. Wu, "A 1.0 V 45nm Nonvolatile Magnetic Latch Design and Its Robustness Analysis," *IEEE Custom Integrated Circuits Conference (CICC)*, September 2011, pages 1-4. (DOI: 10.1109/CICC.2011.6055392)
- C23. Y. Chen, W.-F. Wong, H. Li and C.-K. Koh, "Design of Processor Caches with Multi-Level Spin-Transfer Torque RAM Cells," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, August 2011, pages 73-78. (DOI: 10.1109/ISLPED.2011.5993610)
- C22. Y.-C. Chen, H. Li, W. Zhang and R. Pino, "3D-HIM: A 3-Dimensional High-Density Interleaved Memory for Bipolar RRAM Design," *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, June 2011, pages 59-64. (DOI: 10.1109/NANOARCH.2011.5941484)
- C21. Y.-C. Chen, H. Li, Y. Chen and R. Pino, "3D-ICML: A 3D Bipolar ReRAM Design with Interleaved Complementary Memory Layers," *Design, Automation & Test in Europe Conference and Exhibition (DATE)*, March 2011, pages 1-4. (DOI: 10.1109/DATE.2011.5763289)
- C20. M. Hu, H. Li, Y. Chen, X. Wang, and R. E. Pino, "Geometry Variations Analysis of TiO₂-based and Spintronic Memristors," *the 16th Asia and South Pacific Design Automation Conference (ASPDAC)*, January 2011, pages 25-30. **(Best Paper Nomination, 1 out of 28 in track, 3.6%)** (DOI: 10.1109/ASPDAC.2011.5722193)
- C19. Z. Sun, H. Li, Y. Chen, and X. Wang, "Variation Tolerant Sensing Scheme of Spin-Transfer Torque Memory for Yield Improvement", *International Conference on Computer Aided Design (ICCAD)*, November 2010, pages 432-437. (DOI: 10.1109/ICCAD.2010.5653720)
- C18. Y. Chen, H. Li, X. Wang, W. Zhu, W. Xu and T. Zhang, "Combined Magnetic- and Circuit-level Enhancements for the Nondestructive Self-Reference Scheme of STT-RAM," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, August 2010, pages 1-6. **(Best Paper Award, 3 out of 300, 1%)** (DOI: 10.1145/1840845.1840847)
- C17. Y. Chen, H. Li, Z. Sun, X. Wang, W. Zhu, G. Sun and Y. Xie, "Access Scheme of Multi-Level Cell Spin-

- Transfer Torque Random Access Memory and Its Optimization,” *the 53rd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2010, pages 1109-1112. (DOI: 10.1109/MWSCAS.2010.5548848)
- C16. Y. Chen, W. Tian, H. Li, X. Wang, and W. Zhu, “Scalability of PCMO-based Resistive Switch Device in DSM Technologies”, *International Symposium on Quality Electronic Design (ISQED) 2010*, pages 327-332. **(Best Paper Nomination, 9 out of 245, 3.7%)** (DOI: 10.1109/ISQED.2010.5450447)
- C15. Y. Chen, H. Li, X. Wang, W. Zhu, W. Xu, and T. Zhang, “A Nondestructive Self-Reference Scheme for Spin-Transfer Torque Random Access Memory (STT-RAM)”, *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Dresden, Germany, March 2010, pages 148-153. **(Best Paper Nomination, 20 out of 981 submissions, 2.0%)** (DOI: 10.1109/DATE.2010.5457219)
- C14. G. Sun, Y. Joo, Y. Chen, Y. Xie, Y. Chen, and H. Li, “A Hybrid Solid-State Storage Architecture for the Performance, Energy Consumption, and Lifetime Improvement,” *International Symposium on High-Performance Computer Architecture (HPCA)*, January 2010, pages 141-152. (DOI: 10.1109/HPCA.2010.5416650)
- C13. C.-K. Koh, W.-F. Wong, Y. Chen, and H. Li, “The Salvage Cache: A Fault-tolerant Cache Architecture for Next-generation Memory Technologies,” *IEEE International Conference on Computer Design (ICCD)*, October 2009, pages 268-274. (DOI: 10.1109/ICCD.2009.5413145)
- C12. H. Li, H. Xi, Y. Chen, X. Wang, and T. Zhang, “Thermal-Assisted Spin Transfer Torque Memory (STT-RAM) Cell Design Exploration”, *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2009, pages 217-222. (DOI: 10.1109/ISVLSI.2009.17)
- C11. X. Dong, X. Wu, G. Sun, Y. Chen, H. Li and Y. Xie, “Circuit and Microarchitecture Evaluation of Magnetic RAM (MRAM) as a Universal Memory Replacement”, *Proceedings of the 45th Annual Design Automation Conference (DAC)*, June 2008, pages 554-559. (DOI: 10.1145/1391469.1391610)
- C10. Y. Chen, X. Wang, H. Li, H. Liu and D. Dimitrov, “Design Margin Exploration of Spin-Torque Transfer RAM (SPRAM)”, *International Symposium on Quality Electronic Design (ISQED)*, March 2008, pages 684-690. **(Best Paper Award, 3 out of 300 submissions, 1%)** (DOI: 10.1109/ISQED.2008.4479820)
- C9. C.-K. Koh, W.-F. Wong, Y. Chen, and H. Li, “VOSCH: Voltage Scaled Cache Hierarchies”, *International Conference on Computer Design (ICCD)*, October 2007, pages 496-503. (DOI: 10.1109/ICCD.2007.4601944)
- C8. Y. Chen, H. Li, J. Li and C.-K. Koh, “Variable-latency Adder (VL-Adder): New Arithmetic Circuit Design Practice to Overcome NBTP”, *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, 2007, pages 195-200. (DOI: 10.1145/1283780.1283822)
- C7. H. Li, Y. Chen, K. Roy and C.-K. Koh, “SAVS: A Self-adaptive Variable Supply-voltage Technique for Process-tolerant and Power-efficient Multi-issue Superscalar Processor Design”, *Asia and South Pacific Design Automation Conference (ASP-DAC)*, January 2006, pages 158-163. (DOI: 10.1109/ASPDAC.2006.1594675)
- C6. Y. Chen, H. Li, K. Roy and C.-K. Koh, “Gated Decap: A Technique to Reduce Gate Leakage in Decoupling Capacitors in Scaled Technologies,” *IEEE Custom Integrated Circuits Conference (CICC)*, September 2005, pages 775-778. (DOI: 10.1109/CICC.2005.1568783)
- C5. Y. Chen, H. Li, K. Roy and C.-K. Koh, “Cascaded Carry-Select Adder (C²SA): A New Structure for Low-Power CSA Design”, *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, August 2005, pages 115-118. (DOI: 10.1109/LPE.2005.195498)
- C4. H. Li, C.-Y. Cher, T. N. Vijaykumar, and K. Roy, “VSV: L2-Miss-Driven Variable Supply-Voltage Scaling for Low Power”, *Proceedings of the 36th annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2003, pages 19-28. (DOI: 10.1109/MICRO.2003.1253180)
- C3. H. Li, S. Bhunia, Y. Chen, T. N. Vijaykumar, and K. Roy, “Deterministic Clock Gating for Microprocessor Power Reduction”, *the 9th International Symposium on High-Performance Computer Architecture (HPCA)*, February 2003, pages 113-122. (DOI: 10.1109/HPCA.2003.1183529)
- C2. S. Bhunia, H. Li, and K. Roy, “A High Performance IDDQ Testable Cache for Scaled CMOS Technologies,” *Proceedings of the 11th Asian Test Symposium (ATS)*, November 2002, pages 157-162. (DOI: 10.1109/ATS.2002.1181704)
- C1. A. Agrawal, H. Li, and K. Roy, “DRG-Cache: A Data Retention Gated-Ground Cache for Low Power,” *the 39th Design Automation Conference (DAC)*, June 2002, pages 473-478. (DOI: 10.1109/DAC.2002.1012671)

(v) Peer Reviewed Conference Abstracts and Workshop Publications

- Cw26. H. Li, B. Liu, X. Liu, M. Mao, Y. Chen, Q. Wu, and Q. Qiu, "The Applications of Memristor Devices in Next-generation Cortical Processor Designs," *International Workshop on Neuromorphic and Brain-Based Computing Systems (NeuComp)* collocated with *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Grenoble, France, March 2015.
- Cw25. B. Liu, T. Huang, Q. Wu, M. Barnell, X. Li, and Y. Chen, "Reduction and IR-drop Compensations Techniques for Reliable Neuromorphic Computing," *International Workshop on Design Automation for Analog and Mixed-Signal Circuits* in conjunction with *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, November 2014.
- Cw24. Y.-C. Cheng, C. Yang, and H. Li, "Evaluation of In-place Logic Obfuscation Proposed for ReRAM FPGA," Selected in to the Final Phase in Embedded Security Challenge (ESC) during NYU's CyberSecurity Awareness Week (CSAW), 2014.
- Cw23. E. Eken, Y. Zhang, W. Wen, R. Joshi, H. Li, Y. Chen, "A New Field-assisted Access Scheme of STT-RAM with Self-reference Capability," *IEEE International Magnetics Conference (InterMag)*, Dresden, Germany, May 2014, CC-09.
- Cw22. F. Mao, Y.-C. Chen, W. Zhang, and H. Li, "BMP: A Fast B*-Tree based Modular Placer for FPGAs," *the ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, Monterey, CA, February 2014.
- Cw21. H. Liang, Y.-C. Chen, W. Zhang, and H. Li, "Hierarchical Library-Based Power Estimator for Versatile FPGAs," *the ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, Monterey, CA, February 2014.
- Cw20. M. Hu and H. Li, "The Stochastic Characteristics of Memristor Devices and Case Studies in Neuromorphic Hardware Design," *International Semiconductor Device Research Symposium (ISDRS)*, Maryland, December 2013.
- Cw19. Y. Zhang, I. Bayram, Y. Wang, H. Li, and Y. Chen, "ADAMS: Asymmetric Differential STT-RAM Cell Structure for Reliable and High-performance Applications," *International Workshop on Design Automation for Analog and Mixed-Signal Circuits* in conjunction with *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, November 2013.
- Cw18. X. Chen and H. Li, "P-Spectrum: A Personalized Smartphone Power Management Technique based on Real-time Battery and User Behavior Monitoring," *the 50th Design Automation Conference (DAC)*, Austin, TX, June 2013. (*Work-in-progress Session*)
- Cw17. J. Guo, G. Sun, J. Xue, and H. Li, "The Detection of Malicious Data Attack on NAND Flash Storage System based on Power Signature," *the 50th Design Automation Conference (DAC)*, Austin, TX, June 2013. (*Work-in-progress Session*)
- Cw16. M. Hu, H. Li, G. Rose, Q. Wu, and Y. Chen, "Training Scheme Analysis for Memristor-Based Neuromorphic Design," *International Workshop on Neuromorphic and Brain-Based Computing Systems (NeuComp)* collocated with *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Grenoble, France, March 2013.
- Cw15. M. Mao, H. Li, A. Jones, J. Xue and Y. Chen, "Dynamic Prefetch Aggressiveness Tuning for STT-RAM-based Last-level Cache," *the 4th Workshop on SoCs, Heterogeneous Architectures and Workloads (SHAW4)*, in conjunction with *International Symposium on High-Performance Computer Architecture (HPCA)*, Shenzhen, China, February 2013.
- Cw14. M. Hu and H. Li, "Low Power Neuromorphic Circuit Using Memristor Crossbar Array," *ACM Student Research Competition at the 49th Design Automation Conference (DAC)*, San Francisco, CA, 2012.
- Cw13. X. Bi, H. Li, and X. Wang, "STT-RAM Design Considering Temperature Impact," *IEEE International Magnetics Conference (InterMag)*, Vancouver, Canada, May 2012, FD-12.
- Cw12. Y.-C. Chen, H. Li, and W. Zhang, "A RRAM-based Memory System and Applications," *The Non-Volatile Memories Workshop (NVMW)*, San Diego, CA, March 2012.
- Cw11. Z. Sun, X. Bi, H. Li, W.-F. Wong, X. Zhu, and W. Wu, "Multi Nonvolatility Level STTRAM Cache Hierarchy," *The Non-Volatile Memories Workshop (NVMW)*, San Diego, CA, March 2012.
- Cw10. X. Bi, H. Li, and X. Wang, "Design Considerations for Thermal-assistant STT-RAM through Joule Heating," *the 56th Magnetism and Magnetic Materials Conference (MMM)*, Scottsdale, AZ, October 2011, AF-06.

- Cw9. Z. Sun, H. Li, and X. Wang, "MTJ Design Margin Exploration for Self-Reference Sensing," *the 56th Magnetism and Magnetic Materials Conference (MMM)*, Scottsdale, AZ, October 2011, AF-14.
- Cw8. M. Hu, H. Li, Y. Chen and R. E. Pino, "Statistical Model of TiO₂ Memristor," *the 48th Annual Design Automation Conference (DAC)*, San Diego, CA, June 2011. (*Work-in-progress Session*)
- Cw7. H. Li, X. Wang, Z.-L. Ong, W.-F. Wong, Y. Zhang, P. Wang and Y. Chen, "Performance, Power and Reliability Tradeoffs of STT-RAM Cell Subjective to Architecture-level Requirement," *IEEE International Magnetism Conference (InterMag)*, Taiwan, April 2011, AD-02.
- Cw6. Y. Zhang, X. Wang, H. Li and Y. Chen, "STT-RAM Cell Optimization Considering Process Variations," *IEEE International Magnetism Conference (InterMag)*, Taiwan, April 2011, CC-05.
- Cw5. P. Wang, X. Wang, Y. Zhang, H. Li and Y. Chen, "Spin-MOS Logic and Storage Circuitry Optimization for Non-persistent Error Rate Reduction," *IEEE International Magnetism Conference (InterMag)*, Taiwan, April 2011, FR-01.
- Cw4. Y. Zhang, Y. Chen, X. Wang, H. Li, "STT-RAM Cell Optimization Considering Process Variations," *The Non-Volatile Memories Workshop (NVMW)*, San Diego, CA, March 2011.
- Cw3. Y. Chen, X. Wang, W.-F. Wong, H. Li, "Performance, Power and Reliability Tradeoffs of STT-RAM Cell Subjective to Architecture-level Requirement," *The Non-Volatile Memories Workshop (NVMW)*, San Diego, CA, March 2011.
- Cw2. Z. Sun, H. Li, Y. Chen, and X. Wang, "Magnetic Bio-sensing based on Spintronic Memristor," *International Workshop on Biomedical System Design* collocated with *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, November 2010.
- Cw1. X. Wang, Y. Chen, H. Li, H. Liu and D. Dimitrov, "Spin Torque Random Access Memory down to 22nm Technology", *IEEE International Magnetism Conference (InterMag)*, Madrid, Spain, May 2008, GD-03.

(vi) Invited Conference Publications

- Ci23. H. Li, B. Liu, X. Liu, M. Mao, Y. Chen, Q. Wu, and Q. Qiu, "The Applications of Memristor Devices in Next-generation Cortical Processor Designs," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Portugal, 2015.
- Ci22. Y. Wang, T. Tang, L. Xia, B. Li, P. Gu, H. Li, Y. Xie, and H. Yang, "Energy Efficient RRAM Spiking Neural Network for Real Time Classification," *Proceedings of the 25th ACM International Conference on Great Lakes Symposium on VLSI (GLSVLSI)*, May 2015.
- Ci21. Y. Zhang, B. Yan, W. Wu, H. Li, and Y. Chen, "Giant Spin Hall Effect (GSHE) Logic Design for Low Power Application," *Design, Automation, & Test in Europe*, France, March 2015. (DOI: 10.7873/DATE.2015.1118)
- Ci20. H. Li, X. Liu, M. Mao, Y. Chen, Q. Wu, and M. Barnell, "Neuromorphic Hardware Acceleration Enabled by Emerging Technologies," *the International Symposium on Integrated Circuits (ISIC)*, Singapore, December 2014, pages 124-127. (DOI: 10.1109/ISICIR.2014.7029530)
- Ci19. T. Tang, B. Li, Y. Wang, R. Luo, and H. Li, "Energy Efficient Spiking Neural Network Design with RRAM Devices," *the International Symposium on Integrated Circuits (ISIC)*, Singapore, December 2014, pages 268-271. (DOI: 10.1109/ISICIR.2014.7029565)
- Ci18. Q. Qiu, Z. Li, K. Ahmed, H. Li, and M. Hu, "Neuromorphic Acceleration for Context Aware Text Image Recognition," *IEEE International Workshop on Signal Processing Systems (SiPS)*, UK, October, 2014, pages 1-6. (DOI: 10.1109/SiPS.2014.6986098)
- Ci17. H. Li, M. Hu, X. Liu, M. Mao, C. Li, and S. Duan, "Emerging Memristor Technology Enabled Next Generation Cortical Processor," *the 27th IEEE International SoC Conference (SoCC)*, Las Vegas, NV, September 2014. (DOI: 10.1109/SOCC.2014.6948958)
- Ci16. H. Li, M. Hu, C. Li, and S. Duan, "Memristor Modeling – Static, Statistical, and Stochastic Methodologies," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Tampa, FL, July 2014. (DOI: 10.1109/ISVLSI.2014.108)
- Ci15. Q. Wu, B. Liu, Y. Chen, H. Li, Q. Chen, and Q. Qiu, "Bio-Inspired Computing with Resistive Memories – Models, Architectures and Applications," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Australia, June 2014. (DOI: 10.1109/ISCAS.2014.6865265)
- Ci14. B. Liu, M. Hu, H. Li, Y. Chen and J. Xue, "Bio-inspired Ultra Lower-power Neuromorphic Computing Engine for Embedded Systems," *International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Oct. 2013. (DOI: 10.1109/CODES-ISSS.2013.6659010)

- Ci13. H. Li, Z. Sun, X. Bi, and B. Wysocki, "Spintronic Devices: from Memory to Memristor," *IEEE 11th International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, October 2012, pages 1-4. (DOI: 10.1109/ICSICT.2012.6467793)
- Ci12. H. Li, "Memristor in Neuromorphic Computing," *the 25th IEEE International SoC Conference (SoCC)*, September 2012, pages 294. (DOI: 10.1109/SOCC.2012.6398367)
- Ci11. X. Bi, H. Li, and J.-J. Kim, "Analysis and Optimization of Thermal Effect on STT-RAM Based 3-D Stacked Cache Design," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, August 2012, pp. 374-379. (DOI: 10.1109/ISVLSI.2012.56)
- Ci10. R. E. Pino, H. Li, Y. Chen, *M. Hu, and B. Liu, "Statistical Memristor Modeling and Case Study in Neuromorphic Computing," *Proceedings of the 49th Annual Design Automation Conference (DAC)*, June 2012, pages 585-590. (DOI: 10.1145/2228360.2228466)
- Ci9. R. Joshi, R. Kanj, P. Wang, and H. Li, "Universal Statistical Cure For Predicting Memory Loss", *2011 IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, November 2011, pages 236-239. (DOI: 10.1109/ICCAD.2011.6105333)
- Ci8. J. Xue, Y. Zhang, Y. Chen, G. Sun, J. J. Yang, and H. Li, "Emerging Non-Volatile Memories: Opportunities and Challenges," *ACM Proceedings of the 7th IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS'11)*, October 2011, pages 325-334. (DOI: 10.1145/2039370.2039420)
- Ci7. Y. Chen, and H. Li, "Emerging Sensing Techniques for Emerging Memories," *the 16th Asia and South Pacific Design Automation Conference (ASPDAC)*, January 2011, pages 204-210. (DOI: 10.1109/ASPDAC.2011.5722185)
- Ci6. Y. Chen, X. Wang, H. Li, and J. Park, "Applications of TMR Devices in Solid State Circuits and Systems," *International SoC Design Conference (ISOCC)*, November 2010, pages 252-255. (DOI: 10.1109/SOCC.2010.5682923)
- Ci5. Y. Chen, X. Wang, Z. Sun, and H. Li, "The Application of Spintronic Devices in Magnetic Biosensing", *the 2nd Asia Symposium on Quality Electronic Design (ASQED)*, August 2010, pages 230-234. (DOI: 10.1109/ASQED.2010.5548244)
- Ci4. H. Li and Y. Chen, "Emerging Non-Volatile Memory Technologies – From Materials, to Device, Circuit, and Architecture," *the 53rd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2010, pages 1-4. (DOI: 10.1109/MWSCAS.2010.5548590)
- Ci3. Y. Chen, H. Li, and X. Wang, "Spintronic Devices: from Memory to Memristor," *International Conference on Communications, Circuits and Systems (ICCCAS)*, July 2010, pages 961-963. (DOI: 10.1109/ICCCAS.2010.5581868)
- Ci2. H. Li and M. Hu, "Compact Model of Memristors and Its Application in Computing Systems," *Design, Automation & Test in Europe Conference and Exhibition (DATE)*, March 2010, pages 673-678. (DOI: 10.1109/DATE.2010.5457115)
- Ci1. H. Li and Y. Chen, "An Overview of Non-Volatile Memory Technology and the Implication for Tools and Architectures", *Design, Automation & Test in Europe Conference and Exhibition (DATE)*, 2009, pages 731-736. (DOI: 10.1109/DATE.2009.5090761)

G. INVITED PRESENTATIONS, TUTORIALS, SEMINARS, AND OTHERS

- Tk52. "Neuromorphic Hardware Acceleration Enabled by Emerging Technologies," *the International Symposium on Integrated Circuits (ISIC)*, Singapore, December 10-12, 2014.
- Tk51. "Nonvolatile TCAM Circuit Design Based on Spintronic Technology", Cisco Systems, Milpitas, CA, November 7, 2014.
- Tk50. "Energy Efficiency and Low Power -Circuit, Architecture, System Designs and Applications", Huawei Silicon Valley Site, Cupertino, CA, November 6, 2014.
- Tk49. "Neuromorphic Computing Systems based on Memristor Crossbar Structure," HP Labs, Palo Alto, CA, October 13, 2014.
- Tk48. "Emerging Memristor Technology Enabled Next Generation Cortical Processor," *the IEEE International System-on-Chip Conference (SOCC)*, Las Vegas, Nevada, September 2-5, 2014.
- Tk47. "Memristor Modeling — Static, Statistical, and Stochastic Methodologies," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Tampa, Florida, USA, July 9-11, 2014.
- Tk46. "Design Challenges in MLC STT-RAM Caches," Institute of Computing Technology, Chinese Academy of

- Sciences, July 8, 2014.
- Tk45. “Cross-Layer Racetrack Memory Design for Ultra High Density and Low Power Consumption,” Beihang University, Beijing, China, July 7, 2014.
- Tk44. “Phase Change Memory, Resistive Memory, and Memristor,” School of Information Science and Technology, University of Chinese Academy of Sciences, Beijing, China, June 27, 2014.
- Tk43. “Von Neumann and Neuromorphic Systems Leveraging the Emerging Nonvolatile Devices,” Tsinghua University, June 26, 2014.
- Tk42. “Unleashing the Potential of Multi-level Cells in STT-RAM Caches,” *CRAW/CDC Discipline Specific Workshop on Diversity in Design Automation Conference (DAC)*, San Francisco, CA, May 31, 2014.
- Tk41. “Von Neumann & Neuromorphic Systems atop Spintronic and Resistive Devices,” Department of Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, PA, February 19, 2014.
- Tk40. “Emerging Technology Enabled Next Generation Cortical Processor,” *Machine Intelligence from Cortical Networks (MICrONS) workshop*, Arlington, Virginia, February 11-12, 2014.
- Tk39. “Next-generation Array & Tape Organizations for Revolutionary Spintronic,” Department of Computer Science, School of Computing, National University of Singapore, January 2014.
- Tk38. “Emerging Memristor Technology and Its Usage in Neuromorphic Systems,” School of Electronic Science and Engineering, Nanjing University, December 2013.
- Tk37. “The Stochastic Characteristics of Memristor Devices and Case Studies in Neuromorphic Hardware Design,” *International Semiconductor Device Research Symposium (ISDRS)*, Maryland, December 2013.
- Tk36. “Neuromorphic Systems atop Emerging Devices,” National Cheng Kung University, November 2013.
- Tk35. “Design Space Exploration and Applications of STT-RAM in Modern Computing Systems,” Cisco Inc., November 2013.
- Tk34. “Terminator: Next-generation Array and Tape Organizations for Revolutionary Spintronic,” *EDA Workshop 2013*, Kyoto Research Park, Kyoto, Japan, September 2013.
- Tk33. “General Realization of Neuromorphic Computing Systems Based on Stochastic Characteristics of Memristive Switches,” Air Force Research Lab (AFRL), Rome, August 2013.
- Tk32. “An Adaptive Information Processing System Resilient to Device Variations and Noises,” DARPA, Arlington, VA, August 2013
- Tk31. “Terminator: Next-generation Array and Tape Organizations for Revolutionary Spintronic,” *the 5th International Workshop on Emerging Circuits and Systems (IWECS)*, Chengdu, China, July 25, 2013.
- Tk30. “Terminator: Next-generation Array and Tape Organizations for Revolutionary Spintronic,” *Cloud, Storage, Big Data Summit* jointly held with *the 2nd Asian Nonvolatile Memory Workshop (ANVMW)*, Shanghai, China, July 2013.
- Tk29. Tutorial on “Von Neumann & Neuromorphic Systems atop Spintronic and Resistive Devices,” Qualcomm Inc., San Diego, CA, March 2013.
- Tk28. “Stay Spinning, Stay Cool!” Department of Computer Science, City University of Hong Kong, Hong Kong, March 2013.
- Tk27. “Spintronic Devices: from Memory to Memristor,” on *IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Xi’an, China, November 1, 2012.
- Tk26. Tutorial on “Memristor in Neuromorphic Computing” on *the 25th IEEE International SoC Conference (SoCC)*, Niagara Fall, NY, September 2012.
- Tk25. “Runtime Programmable FPGA Architecture based on Nanoscale RRAM,” on *Network Science and Reconfigurable Systems for Cyber Security (NSRSC) Conference*, Washington DC, August 29, 2012.
- Tk24. “Evolution or Revolution: NVM-enabled Transition from von Neumann Architecture to Neuromorphic Hardware,” Department of Computer Science, School of Computing, National University of Singapore, August 8, 2012.
- Tk23. “Stay Spinning, Stay Cool!” A*STAR Data Storage Institute (DSI), Singapore, July 26, 2012.
- Tk22. “STT-RAM Research of Pitts and NYU-Poly Team,” at the Samsung Memory Division, Dongtan, Korea, July 6, 2012.
- Tk21. Summer Short Courses on “Emerging Memory Design and Applications,” Tsinghua University, June 25 – July 3, 2012.

- Tk20. “Probabilistic Design to Improve Runtime Stability and Performance of STT-RAM,” IBM T. J. Watson, NY, March 2012.
- Tk19. “An Overview of STT-RAM Technology – from Device Modeling to Applications,” Princeton/Central New Jersey Chapter of the IEEE SSCS (Solid-State Circuits Society) Chapter, Rutgers University, Piscataway, NJ, November 2011.
- Tk18. Tutorial on “Spintronic Devices – the Future Storage and Computing Elements in Computing Systems,” *International ASIC Conference (ASICON)*, October 2011.
- Tk17. Tutorial on “STT-RAM Technology: Device, Circuit, and System Applications,” Qualcomm Inc., San Diego, CA, September 2011.
- Tk16. “Memristor-Based Reconfigurable Design for Neuromorphic Computing Architecture,” Air Force Research Lab (AFRL), Rome, NY, August 2011.
- Tk15. Tutorial on “STT-RAM Technology: Device, Circuit, Architecture and Applications,” Avalanche Inc., Fremont, CA, August 2011.
- Tk14. “Memristor-Based 3D Neuromorphic Computing Architectures,” *Workshop on Future Perspectives of Neuromorphic Memristor Science & Technology*, collocated with *International Joint Conference on Neural Networks (IJCNN)*, San Jose, CA, July 2011.
- Tk13. “Integrating Emerging Memory on Top of CMP: Opportunities and Challenge,” *D43D: the 4th Design for 3D Silicon Integration Workshop*, MINATEC, Grenoble, France, June 2011.
- Tk12. “Memristor and Its Applications in Neuromorphic and Reconfigurable Computing Platform,” Air Force Research Lab (AFRL), Dayton, OH, June 2011.
- Tk11. Tutorial on “Application of Spintronic for MRAM and Memristor-based Computing,” *International Symposium on Quality Electronic Design (ISQED)*, San Jose, CA, March 2011.
- Tk10. “Emerging Sensing Techniques for Emerging Memories,” *the 16th Asia and South Pacific Design Automation Conference (ASP-DAC)*, January 2011.
- Tk9. “Memristor-Based Computing Architecture: Design Methodology & Circuit Techniques,” Boise State University, January 2011.
- Tk8. “Emerging Non-Volatile Memory Technologies – From Materials, to Device, Circuit, and Architecture,” *the 53rd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2010.
- Tk7. “Memristor-Based Computing Architecture: Design Methodology & Circuit Techniques,” Air Force Research Lab (AFRL), Rome, October 2010.
- Tk6. “Compact Model of Memristors and Its Application in Computing Systems,” *Design, Automation & Test in Europe Conference and Exhibition (DATE)*, April 2010.
- Tk5. “Spin-Transfer Torque Random Access Memory – Device, Circuit and Architecture,” Department of Electrical and Computer Engineering, Princeton University, November 2009.
- Tk4. “An Overview of Non-Volatile Memory Technology and the Implication for Tools and Architectures,” *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, April 2009.
- Tk3. “Spin-Transfer Torque Random Access Memory – Next Breakthrough in Embedded System,” Department of Electrical and Computer Engineering, University of California, Santa Barbara, March 2009.
- Tk2. “Emerging Non-volatile Memory: Spin-Transfer Torque Memory and Resistive Memory,” Department of Electronic Engineering, Tsinghua University, December 2008.
- Tk1. “Low-Power Design Technique at Circuit and Microarchitectural Boundary,” *the 7th SIGDA Ph.D. Forum at Design Automation Conference (DAC)*, June 2004.

H. PATENTS

A. Patents Granted

- P72. Y. Chen, H. Li, H. Liu, D. Dimitrov, X. Wang, and X. Wang, “Predictive Pre-heating of Nonvolatile Memory Cells,” EP 2415051. (**International Patent**)
- P71. H. Li, Y. Chen, H. Liu, K.-Y. Kim, D. Dimitrov, and H. Huang, “Spin-transfer Torque Memory Self-reference Read Method,” US Patent 8,675,401, approved on March 18, 2014.
- P70. H. Li, Y. Chen, H. Liu and H. Huang, “Non-volatile Resistive Sense Memory On-Chip Cache,” US Patent 8,650,355, approved on February 11, 2014.

- P69. Y. Chen, H. Li, H. Liu, D. Dimitrov, X. Wang, and X. Wang, "Predictive Thermal Preconditioning and Timing Control for Non-volatile memory Cells," US Patent 8,553,454, approved on October 8, 2013.
- P68. H. Li, Y. Chen, Y. Yan, B. Lee, and R. Wang "Dual Stage Sensing for Non-volatile Memory," US Patent 8,537,587, approved on September 17, 2013.
- P67. H. Li, Y. Chen, A. Wang, H. Xi, W. Zhu, and A. Roelofs, "Quiescent Testing of Non-volatile Memory Array," US Patent 8,526,252, approved on September 3, 2013.
- P66. Y. Chen, H. Li, W. Zhu, X. Wang, H. Wang, and H. Liu, "Spatial Correlation of Reference Cells in Resistive Memory Array," US Patent 8,526,215, approved on September 3, 2013.
- P65. Y. Chen, H. Li, H. Liu, Y. Lu, and S. Xue, "MRAM Diode Array and Access Method," US Patent 8,514,605, approved on August 20, 2013.
- P64. X. Wang, Y. Lu, H. Li, and H. Liu, "Three Dimensionally Stacked Non-volatile Memory Unit," US Patent 8,482,957, approved on July 9, 2013.
- P63. M. Sun, N. Amin, I. Jin, Y. -P. Kim, C. Jung, V. Vaithyanathan, W. Tian, and H. Li, "Programmable Metallization Cell Switch and Memory Units Containing the Same," US Patent 8,446,752, approved on May 21, 2013.
- P62. Y. Chen, H. Li, H. Liu, Y. Lu and Y. Li, "Transmission Gate-Based Spin-Transfer Torque Memory Unit," US Patent 8,416,615, approved on April 9, 2013.
- P61. Y. Chen, H. Li, H. Liu, R. Wang, and D. Dimitrov, "Spin-transfer Torque Memory Non-destructive Self-reference Read Method," US Patent 8,416,614, approved on April 9, 2013.
- P60. H. Li, Y. Chen, H. Liu, K.-Y. Kim, D. Dimitrov, and H. Huang, "Spin-transfer Torque Memory Self-reference Read Method," US Patent 8,411,495, approved on April 2, 2013.
- P59. X. Wang, Y. Chen, X. Wang, H. Xi, W. Zhong, H. Li, and H. Liu, "Magnetic Tunnel Junction and Memristor Apparatus," US Patent 8,391,055, approved on March 5, 2013.
- P58. Y. Chen, H. Li, H. Liu, Y. Lu, and S. Xue, "Data Devices Including Multiple Error Correction Codes and Methods of Utilizing," US Patent 8,296,620, approved on October 23, 2012.
- P57. H. Huang, H. Li, and Y. Lu, "Data Storage Using Read-Mask-Write Operation," US Patent 8,289,786, approved on October 18, 2012.
- P56. Y. Chen, H. Li, H. Liu, Y. Lu, and S. Xue, "MRAM Diode Array and Access Method," US Patent 8,289,746, approved on October 16, 2012.
- P55. D. Reed, Y. Lu, A. Carter, and H. Li, "Non-Volatile Memory Array with Resistive Sense Element Block Erase and Uni-Directional Write," US Patent 8,213,259, approved on July 3, 2012.
- P54. X. Wang, H. Li, and H. Liu, "Shared Bit Line and Source Line Resistive Sense Memory Structure," US Patent 8,213,216, approved on July 3, 2012.
- P53. Y. Chen, H. Li, W. Zhu, X. Wang, H. Huang, and H. Liu, "Resistive Sense Memory Calibration for Self-Reference Read Method," US Patent 8,213,215, approved on July 3, 2012.
- P52. Y. Chen, H. Li, W. Zhu, X. Wang, R. Wang, and H. Liu, "Memory Cell with Proportional Current Self-Reference Sensing," US Patent 8,203,899, approved on June 19, 2012.
- P51. H. Li, Y. Chen, H. Liu, H. Huang and R. Wang, "Write Current Compensation Using Word Line Boosting Circuitry," US Patent 8,203,893, approved on June 19, 2012.
- P50. Y. Chen, H. Li, W. Zhu, X. Wang, Y. Yan, and H. Liu, "Voltage Reference Generation with Selectable Dummy Regions," US Patent 8,203,862, approved on June 19, 2012.
- P49. Y. Chen, H. Li, H. Liu, Y. Lu and Y. Li, "Transmission Gate-Based Spin-Transfer Torque Memory Unit," US Patent 8,199,563, approved on June 12, 2012.
- P48. W. Zhu, H. Li, Y. Chen, X. Wang, H. Huang, and H. Xi, "Memory Cell with Enhanced Read and Write Sense Margins," US Patent 8,199,562, approved on June 12, 2012.
- P47. Y. Chen, D. Reed, Y. Lu, H. Liu, and H. Li, "Computer Memory Device with Multiple Interfaces," US Patent 8,194,437, approved on June 5, 2012.
- P46. Y. Chen, H. Li, H. Liu, D. Dimitrov, X. Wang, and X. Wang, "Predictive Thermal Preconditioning and Timing Control for Non-volatile memory Cells," US Patent 8,154,914, approved on April 10, 2012.
- P45. Y. Chen, H. Li, W. Zhu, X. Wang, H. Wang, and H. Liu, "Spatial Correlation of Reference Cells in Resistive Memory Array," US Patent 8,139,397, approved on March 20, 2012.
- P44. Y. Chen, H. Li, H. Liu, R. Wang, and D. Dimitrov, "Spin-transfer Torque Memory Non-destructive Self-reference Read Method," US Patent 8,116,123, approved on February 14, 2012.

- P43. H. Li, Y. chen, H. Liu, K.-Y. Kim, D. Dimitrov, and H. Huang, "Spin-transfer Torque Memory Self-reference Read Method," US Patent 8,116,122, approved on February 14, 2012.
- P42. H. Li, Y. Chen, H. Liu and X. Wang, "Static Source Plane in STRAM," US Patent 8,098,516, approved on January 17, 2012.
- P41. H. Liu, Y. Lu, A. Carter, Y. Chen, H. Li, and H. Xi, "Memory Array with Read Reference Voltage Cells," US Patent 8,098,513, approved on January 17, 2012.
- P40. Y. Chen, D. Reed, Y. Lu, H. Liu, and H. Li, "Computer Memory Device with Status Register," US Patent 8,081,504, approved on December 20, 2011.
- P39. H. Li, Y. Chen, H. Liu and X. Wang, "Static Source Plane in ST-RAM," US Patent 8,068,359, approved on November 29, 2011.
- P38. X. Wang, Y. Chen, X. Wang, H. Xi, W. Zhong, H. Li, and H. Liu, "Magnetic Tunnel Junction and Memristor Apparatus," US Patent 8,059,453, approved on November 15, 2011.
- P37. A. Wang, X. Wang, D. Dimitrov, H. Li, H. Xi, and H. Liu, "Stuck-at Defect Condition Repair for A Non-volatile Memory Cell," US Patent 8,054,678, approved on November 8, 2011.
- P36. H. Xi, H. Liu, X. Wang, Y. Lu, Y. Chen, Y. Zheng, D. V. Dimitrov, D. Wang, and H. Li, "Variable Write and Read Methods for Resistive Random Access Memory," US Patent 8,054,675, approved on November 8, 2011.
- P35. X. Wang, Y. Lu, H. Li, and H. Liu, "Three Dimensionally Stacked Non-volatile Memory Unit," US Patent 8,054,673, approved on November 8, 2011.
- P34. H. Li, Y. Chen, Y. Yan, B. Lee, and R. Wang "Dual Stage Sensing for Non-volatile Memory," US Patent 8,050,072, approved on November 1, 2011.
- P33. Y. Lu, H. Liu, H. Li, A. J. Carter, D. Reed, and H. Xi, "Multi-Stage Parallel Data Transfer," US Patent 8,045,412, approved on October 25, 2011.
- P32. H. Huang, H. Li and Y. Lu, "Data Storage Using Read-Mask-Write Operation," US Patent 8,040,743, approved on October 18, 2011.
- P31. Y. Chen, D. Reed, Y. Lu, H. Liu, H. Li, and R. Bowman, "Bit Set Modes for a Resistive Sense Memory Cell Array," US Patent 8,040,713, approved on October 18, 2011.
- P30. H. Li, Y. Chen, H. Liu, H. Huang and R. Wang, "Write Current Compensation Using Word Line Boosting Circuitry," US Patent 8,009,457, approved on August 30, 2011.
- P29. H. Li, Y. Chen, H. Liu, H. Huang and R. Wang, "Write Current Compensation Using Word Line Boosting Circuitry," US Patent 7,974,121, approved on July 5, 2011.
- P28. Y. Chen, H. Li, H. Liu, Y. Lu and Y. Li, "Transmission Gate-Based Spin-Transfer Torque Memory Unit," US Patent 7,974,119, approved on July 5, 2011.
- P27. Y. Chen, D. Setiadi, H. Li, H. Xi and H. Liu, "Generic Non-volatile Service Layer," US Patent 7,966,581, approved on June 21, 2011.
- P26. H. Xi, H. Liu, X. Wang, Y. Lu, Y. Chen, Y. Zheng, D. V. Dimitrov, D. Wang, and H. Li, "Variable Write and Read Methods for Resistive Random Access Memory," US Patent 7,952,917, approved on May 31, 2011.
- P25. Y. Chen, D. Reed, Y. Lu, H. Liu, and H. Li, "Resistive Sense Memory Array with Partial Block Update Capability," US Patent 7,944,731, approved on May 17, 2011.
- P24. Y. Chen, H. Li, W. Zhong, X. Wang, and R. Wang, "Write Method with Voltage Line Tuning," US Patent 7,944,730, approved on May 17, 2011.
- P23. Y. Chen, D. Reed, Y. Lu, H. Liu, and H. Li, "Simultaneously Writing Multiple Addressable Blocks of User Data to a Resistive Sense Memory Cell Array," US Patent 7,944,729, approved on May 17, 2011.
- P22. X. Wang, H. Li, and H. Liu, "Shared Bit Line and Source Line Resistive Sense Memory Structure," US Patent 7,940,548, approved on May 10, 2011.
- P21. Y. Chen, H. Li, H. Liu, K. Kim and H. Huang, "Pipeline Sensing Using Voltage Storage Elements to Read Non-volatile Memory Cells," US Patent 7,936,625, approved on May 3, 2011.
- P20. H. Li, Y. Chen, D. Setiadi, H. Liu, and B. Lee, "Defective Bit Scheme for Multi-Layer Integrated Memory Device," US Patent 7,936,622, approved on May 3, 2011.
- P19. H. Liu, Y. Lu, A. Carter, Y. Chen, H. Li, and H. Xi, "Memory Array with Read Reference Voltage Cells," US Patent 7,936,588, approved on May 3, 2011.
- P18. Y. Chen, H. Li, H. Liu, Y. Lu, and S. Xue, "MRAM Diode Array and Access Method," US Patent

- 7,936,580, approved on May 3, 2011.
- P17. Y. Chen, H. Li, H. Liu, D. Dimitrov, X. Wang et. al., “Predictive Thermal Pre-Conditioning and Timing Control for Non-volatile Memory Cells,” US Patent 7,916,528, approved on March 29, 2011.
- P16. H. Li, Y. Chen, H. Liu and X. Wang, “Non-volatile Memory Read/Write Verify,” US Patent 7,916,515.
- P15. X. Wang, Y. Chen, X. Wang, H. Xi, W. Zhong, H. Li, and H. Liu, “Magnetic Tunnel Junction and Memristor Apparatus,” US Patent 7,898,844, approved on March 1, 2011.
- P14. Y. Chen, H. Li, W. Zhu, X. Wang, H. Huang and H. Liu, “Resistive Sense Memory Calibration for Self-Reference Read Method,” US Patent 7,898,838, approved on March 1, 2011.
- P13. A. Wang, X. Wang, D. Dimitrov, H. Li, H. Xi, and H. Liu, “Stuck-at Defect Condition Repair for A Non-volatile Memory Cell,” US Patent 7,894,250, approved on February 22, 2011.
- P12. D. Reed, Y. Lu, A. Carter, and H. Li, “Non-Volatile Memory Array with Resistive Sense Element Block Erase and Uni-Directional Write,” US Patent 7,885,097, approved on February 8, 2011.
- P11. Y. Chen, H. Li, H. Liu, K. Kim and H. Huang, “Voltage Reference Generation for Resistive Sense Memory Cells,” US Patent 7,881,094, approved on February 1, 2011.
- P10. Y. Chen, H. Li, W. Zhu, X. Wang, H. Wang and H. Liu, “Spatial Correlation Aware Reference Level Generation,” US Patent 7,876,599, approved on January 25, 2011.
- P9. H. Li, Y. Chen, H. Liu and X. Wang, “Static Source Plane in ST-RAM,” US Patent 7,859,891, approved on December 28, 2010.
- P8. H. Li, Y. Chen, H. Liu, H. Huang and R. Wang, “Write Current Compensation Using Word Line Boosting Circuitry,” US Patent 7,855,923, approved on December 21, 2010.
- P7. Y. Chen, H. Li, W. Zhu, X. Wang, R. Wang, and H. Liu, “Memory Cell with Proportional Current Self-Reference Sensing,” US Patent 7,852,665, approved on December 14, 2010.
- P6. W. Zhu, H. Li, Y. Chen, X. Wang, H. Huang, and H. Xi, “Enhancing Read and Write Sense Margins in a Resistive Sense Element,” US Patent 7,852,660, approved on December 14, 2010.
- P5. H. Huang, H. Li, and Y. Lu, “Data Storage Using Read-Mask-Write Operation,” US Patent 7,830,726, approved on November 9, 2010.
- P4. Y. Chen, D. Reed, Y. Lu, H. Liu, and H. Li, “Resistive Sense Memory Array with Partial Block Update Capability,” US Patent 7,830,700, approved on November 9, 2010.
- P3. H. Xi, H. Liu, X. Wang, Y. Lu, Y. Chen, Y. Zheng, D. V. Dimitrov, D. Wang, and H. Li, “Variable Write and Read Methods for Resistive Random Access Memory,” US Patent 7,826,255, approved on November 2, 2010.
- P2. Y. Chen, H. Li, H. Liu, H. Huang, Y. Lu, “Temperature Dependent Method of Reading STT-RAM,” US Patent 7,755,965, approved on July 13, 2010.
- P1. H. Liu, Y. Lu, A. Carter, Y. Chen, H. Li, and H. Xi, “Memory Array with Read Reference Voltage Cells,” US Patent 7,755,923, approved on July 13, 2010.

B. Patents Pending

- Pp12. W. Wen, E. Eken, H. Li, X. Bi, and Y. Chen, “Spin-transfer Torque Memory Magnetic-assisted Nondestructive Self-reference Sensing Method,” US Provisional Patent filed.
- Pp11. R. Linderman, Q. Wu, G. Rose, H. Li, Y. Chen, and M. Hu, “Apparatus for Performing Matrix-vector Multiplication Approximation Using Crossbar Arrays of Resistive Memory Devices,” US Patent Pending, 61,848,775, filed on December 19, 2012.
- Pp10. Y. Chen, I. Jin, H. Li, X. Wang, D. Dimitrov, and D. Wang, “Programmable Power Source Using Array of Resistive Sensing Memory Cells,” US Patent Pending, 12/396,126.
- Pp9. Y. Chen, H. Li, W. Zhu, X. Wang, Y. Yan, and H. Liu, “Data Updating in Non-volatile Memory”. US Patent Pending, 12/482,693.
- Pp8. D. Jiao, H. Li, R. Wang, H. Huang, and Y. Chen, “Integrated Circuit Active Power Supply Regulation,” US Patent Pending, 12/501,375.
- Pp7. Y. Chen, H. Li, W. Zhu, X. Wang, Y. Yan, and H. Liu, “XRAM-Based Log Page for Flash Memory,” US Patent Pending, 12/482,693.
- Pp6. Y. Chen, H. Li, H. Liu and X Wang, “Memory Hierarchy with Non-volatile Filter and Victim Caches,” US Patent Pending, 12/332,669.
- Pp5. Y. Chen, H. Li, H. Liu and X. Wang, “Fault Tolerant Non-volatile Buddy Memory Structure,” US Patent Pending, 12/269,535.

- Pp4. Y. Chen, H. Li, H. Liu, H. Xi and S. Xue, "Memory Hierarchy Containing Only Non-volatile Cache," US Patent Pending, 12/198,513.
- Pp3. Y. Chen, H. Li, H. Liu, R. Wang and D. Dimitrov, "Spin-Transfer Torque Memory Non-Destructive Self-Reference Read Method," International Patent Pending, PCT/US09/38935.
- Pp2. H. Li, Y. Chen, X. Wang, and Y. Yan, "Non-volatile Memory Having Increased Sensing Margin," US Patent Pending, 12/500,172.
- Pp1. H. Li, Y. Chen, H. Liu, D. Setiadi and B. Lee, "Pipelined Memory Access Method and Architecture Thereof," US Patent Pending, 12/200,118.

C. Trade Secret

1 trade secret of Seagate Technology LLC.

I. PROFESSIONAL SERVICE ACTIVITIES

(i) University Services

- 1) ECE Undergraduate Committee, University of Pittsburgh, 2013-present.
- 2) ECE Technical Area Committee (Computers), University of Pittsburgh, 2012-present.
- 3) ECE Undergraduate Lab Committee, University of Pittsburgh, 2014-present.
- 4) Graduate Curriculum Committee, Polytechnic Institute of New York University, 2011-2012.
- 5) NYUAD Search Committee, Polytechnic Institute of New York University, 2010-2011.

(ii) IEEE Service

- 1) Technical Committee, Very Large Scale Integration (TCVLSI) of the IEEE Computer Society (IEEE-CS), 2014-

(iii) Journal Editor

- 1) Associate Editor, ACM Transactions on Design Automation of Electronic Systems (TODAES), 2014-
- 2) Associate Editor, IEEE Transactions on Very Large Scale Integration (TVLSI) Systems, 2014-
- 3) Associate Editor, IEEE Transactions on Multi-Scale Computing Systems (TMSCS), 2015-

(iv) Conference/Workshop Organizer

- 1) Local Arrangement Committee, Embedded Systems Weeks (ESWEEK), Pittsburgh PA, October 2016.
- 2) General Chair, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Pittsburgh PA, July 2016.
- 3) Tutorial Chair, IEEE International System-on-Chip Conference (SOCC), Beijing, China, September 2015.
- 4) Program co-chair for SIGDA summer school (DASS), co-located event with Design Automation Conference (DAC), San Francisco, CA, June 2015.
- 5) General Co-chair, Proceedings of the 25th ACM International Conference on Great Lakes Symposium on VLSI (GLSVLSI), Pittsburgh PA, May 2015.
- 6) Tutorial Co-chair, International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, March 2015.
- 7) Finance Chair, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Clearwater FL, July 2014.
- 8) Organizer of special session on "Neuromorphic Science & Technology for Augmented Human Performance in Cybersecurity," International Joint Conference on Neural Networks (IJCNN), Beijing China, July 2014.
- 9) TPC Co-chair, Proceedings of the 24th ACM International Conference on Great Lakes Symposium on VLSI (GLSVLSI), Houston, TX, May 2014.
- 10) Finance Chair, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Amherst MA, August 2012.
- 11) Organizer of special session on "Hardware/Software Co-design for Emerging Nonvolatile Memories," IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Amherst MA, August 2012.
- 12) Organizer of special session on "Emerging Neuromorphic Hardware Architectures and Applications," International Joint Conference on Neural Networks (IJCNN), San Jose CA, July 2011.
- 13) General Co-chair, 3D Integration Workshop for High Performance Computing Systems Workshop, Abu Dhabi, April 18-19, 2011.

- 14) Organizer and coordinator of panel on “Emerging Memory Technology,” IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), San Francisco, CA, July 2009.

(v) Technical Program Track Chair/Co-chair

- 1) The track of “Embedded Systems, Multi/Many Core Systems & Embedded Memory Technologies” in the 27th IEEE International System-on-Chip Conference (SOCC), Las Vegas, NV, September 2014.
- 2) The track of “Logic and Architecture” in International Symposium on Low Power Electronics and Design (ISLPED), San Diego, CA, August 2014.
- 3) The track of “System-level Design and Methodologies (SDM)” in International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, March 2014.
- 4) The track of “Emerging Technologies and Applications” in Asia and South Pacific Design Automation Conference (ASP-DAC), Singapore, January 2014.
- 5) The track of “NVM Device 2” in Cloud, Storage, Big Data Summit jointly held with the 2nd Asian Nonvolatile Memory Workshop (ANVMW), Shanghai, China, July 22, 2013.
- 6) The track of “Logic and Microarchitecture Design” in International Symposium on Low Power Electronics and Design (ISLPED), Beijing, China, September 2013.
- 7) The track of “Post-CMOS VLSI and Emerging Technologies” in Proceedings of the 23rd ACM International Conference on Great Lakes Symposium on VLSI (GLSVLSI), Paris, France, May 2013.
- 8) The track of “Emerging Technologies and Applications” in Asia and South Pacific Design Automation Conference (ASP-DAC), Yokohama, Japan, January 2013.
- 9) The track of “Post-CMOS VLSI” in Proceedings of the 22nd ACM International Conference on Great Lakes Symposium on VLSI (GLSVLSI), Utah, May 2012.
- 10) The track of “MRAM and Magnetic Logic Devices I” in International Magnetics Conference (INTERMAG), Vancouver, Canada, May 2012.

(vi) Technical Program Committee Member

- 1) Design Automation Conference (DAC), 2014-2015.
- 2) International Conference on Computer-Aided Design (ICCAD), 2014.
- 3) International Symposium on Low Power Electronics and Design (ISLPED), 2010-2014.
- 4) Design, Automation & Test in Europe Conference & Exhibition (DATE), 2010-2014.
- 5) Asia and South Pacific Design Automation Conference (ASP-DAC), 2011-2014.
- 6) International Conference on Computer Design (ICCD), 2010-2014.
- 7) International Conference on Great Lakes Symposium on VLSI (GLSVLSI), 2010-2014.
- 8) International Symposium on Quality Electronic Design (ISQED), 2012-2015.
- 9) Asia Symposium on Quality Electronic Design (ASQED), 2009-2013.
- 10) IEEE International SoC Conference (SoCC), 2012-2015.
- 11) Conference on VLSI Design, 2012, 2014.
- 12) International Conference on Embedded Software and Systems (ICCESS), 2015.
- 13) IEEE International Workshop on Signal Processing Systems (SiPS), 2014.
- 14) International Workshop on Non-Volatile Memory (INVM), 2013.
- 15) International Conference on Field Programmable Logic and Applications (FPL), 2008-2010.
- 16) International Conference on Field-Programmable Technology (FPT), 2007-2011.
- 17) IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), 2009-2011.
- 18) IEEE/IFIP International Conference on VLSI and System-on-Chip (VLSI-SoC), 2010.
- 19) IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2009, 2014-2015.
- 20) ACM SIGDA Student Research Competition (SRC) 2011 at Design Automation Conference, 2011.
- 21) IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC), 2011.
- 22) International Symposium on Electronic System Design (ISED), 2010.
- 23) International Congress on Computer Applications and Computational Science (CACCS), 2010.
- 24) World Congress on Nature and Biologically Inspired Computing (NaBIC), 2011.
- 25) International Electronic Design Education Conference (IEDEC), 2012-2014.
- 26) Workshop on Emerging Supercomputing Technologies (In conjunction with International Conference on Supercomputing), 2011.

(vii) Conference/Workshop Session Chair

- 1) International Symposium on Quality Electronic Design (ISQED), 2015.
- 2) International Conference on Computer-Aided Design (ICCAD), November 2014.
- 3) Design Automation Conference (DAC), June 2014.
- 4) International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, March 2014.
- 5) Asia and South Pacific Design Automation Conference (ASP-DAC), Singapore, January 2014.
- 6) Design Automation Conference (DAC), June 2013.
- 7) IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Xi'an, China, November 2012.
- 8) The 25th IEEE International SoC Conference (SoCC), September 2012.
- 9) IEEE International Magnetics Conference (InterMag), Vancouver, Canada, May 2012.
- 10) Design, Automation & Test in Europe Conference & Exhibition (DATE), Dresden, Germany, March 2012.
- 11) International Joint Conference on Neural Networks (IJCNN), San Jose, CA, July 2011.
- 12) Design, Automation & Test in Europe Conference & Exhibition (DATE), Grenoble, France, March 2011.
- 13) Asia and South Pacific Design Automation Conference (ASP-DAC), Yokohama, Japan, January 2011.
- 14) IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), Seattle, WA, August 2010.
- 15) Design, Automation & Test in Europe Conference & Exhibition (DATE), Dresden, Germany, March 2010.
- 16) International Conference on Computer Design (ICCD), Lake Tahoe, CA, October, 2009.
- 17) IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), San Francisco, CA, July 2009.
- 18) International Symposium on Quality Electronic Design (ISQED), San Jose, CA, June 2009.
- 19) IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Tampa, Florida, May 2009.

(vii) Journal/Conference Referee

- 1) IEEE Journal of Solid-State Circuits (JSSC)
- 2) IEEE Transactions on Very Large Scale Integration (VLSI) Systems
- 3) IEEE Transactions on Computers (TC)
- 4) IEEE Transactions on Neural Network and Learning System (TNNLS)
- 5) IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- 6) IEEE Transactions on Electron Devices (TED)
- 7) IEEE Transactions on Nanotechnology (TNANO)
- 8) IEEE Transactions on Information Forensics & Security (T-IFS)
- 9) IEEE Electron Device Letters (EDL)
- 10) IEEE Embedded Systems Letters (ESL)
- 11) ACM Transactions on Architecture and Code Optimization (TACO)
- 12) ACM Journal of Emerging Technologies in Computing (JETC)
- 13) Journal of Circuits, Systems and Computers (JCSC)
- 14) IEEE Design & Test of Computers
- 15) Sensors – Open Access Journal
- 16) Integration, the VLSI Journal (VLSI-D)
- 17) Microprocessors and Microsystems (MICPRO)
- 18) Microelectronics Journal (MEJ)
- 19) The Scientific World Journal
- 20) Neurocomputing (NEUCOM)
- 21) ACM Design Automation Conference (DAC)
- 22) IEEE/ACM International Symposium on Microarchitecture (MICRO)
- 23) International Conference on Computer-Aided Design (ICCAD)
- 24) Design, Automation & Test in Europe (DATE)
- 25) International Joint Conference on Neural Networks (IJCNN)
- 26) IEEE International Symposium on Circuits and Systems (ISCAS)
- 27) IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)
- 28) International Conference on VLSI Design
- 29) European Conference on Circuit Theory & Design (ECCTD)

- 30) IEEE Symposium Series on Computational Intelligence (SSCI)
 31) Neural Computing and Applications (NCAA), Springer

(ix) Other Services

- 1) Panelist for DOE Early Career Research Program (2014)
- 2) Panelist for NSF MRI program (2012-2013)
- 3) Reviewer of 2014 Collaborative Research Grant Competition, Rhode Island Science and Technology Advisory Council (2014)
- 4) Reviewer of Public Sector Funding Research Scheme (PSF) of Science & Engineering Research Council (SERC), the Agency for Science, Technology & Research (A*STAR), Singapore (2011)

J. TEACHING HISTORY

Department of Electrical & Computer Engineering, University of Pittsburgh

ECE 1193/2193	<i>Advanced VLSI Design</i>	2015 Spring
ECE 1192/2192	<i>Introduction to VLSI Design</i>	2014 Fall
CoE 501	<i>Digital System Laboratory</i>	2014 Fall, 2013 Fall
CoE 132	<i>Digital Logic</i>	2014 Spring, 2013 Spring & Fall
ECE 3893	<i>Graduate Seminar</i>	2015 Spring

Department of Electrical & Computer Engineering, Polytechnic Institute of New York University

EL 5473	<i>Introduction to VLSI</i>	2012 Spring & Fall, 2011 Fall, 2010 Spring & Fall
EL 6443	<i>VLSI System and Architecture Design</i>	2012 Spring
EL 5483	<i>Real-Time Embedded System Design</i>	2011 Spring

J. GRADUATE STUDENTS

– *Supervised Post-Doc*

Jianlei Yang Post-Doc., 2014.11-2015.11 (expected)

– *Supervised Students as Primary Advisor* († indicates the students co-supervised with Professor Yiran Chen.)

Zheng Li: Ph.D., 2014.09-2018.07 (expected)
 Wei Wen: Ph.D., 2014.09-2018.07 (expected)
 Chunpeng Wu: Ph.D., 2014.09-2018.07 (expected)
 Chaofei Yang: Ph.D., 2014.09-2018.07 (expected)
 Sicheng Li: Ph.D., 2014.01-2018.01 (expected)
 † Xue Wang: Ph.D., 2014.01-2019.01 (expected)
 Chenchen Liu: Ph.D., 2013.09-2018.07 (expected)
 † Ismail Bayram Ph.D., 2013.01-2017.07 (expected)
 † Mengjie Mao Ph.D., 2012.09-2016.07 (expected)
 Yi-Chung Chen: Ph.D., 2010.01-2013.10 (proposal)-2014.12
 Xiuyuan Bi: Ph.D., 2010.09-2013.06 (proposal)-2014.12 (first job: Marvell Inc.)
 Miao Hu: Ph.D., 2009.09-2013.09 (proposal)-2014.08 (first job: HP Labs)
 Zhenyu Sun: Ph.D., 2010.01-2013.04 (proposal)-2013.12 (first job: Broadcom Corp.)

Sicheng Li: M.S., 2011.09-2013.08 (Continue Ph.D. program in Pitt)
 Feng Ji: M.S., 2011.09-2013.08 (first job: AMD)
 Robert Dunn: M.S., 2011.09-2013.08
 Mohamed A. Weldon: M.S., 2012.01-2013.08
 Yu Bi: M.S., 2011.09-2012.08
 Wenhua Wang: M.S., 2011.05-2012.08 (first job: Standard & Poors)
 Wenzhen Chen: M.S., 2009.09-2010.08 (first job: Marvell Technology Group Ltd.)
 Junjun Liu: M.S., 2010.09-2010.08 (first job: Qualcomm Inc.)
 Sohaib Marie: M.S., 2010.09-2011.08 (first job: Con Edison of New York)

- Weiwei Zhong: M.S., 2010.09-2011.08(first job: Tensorcom Inc.)
Hui Wang: M.S., 2010.01-2011.08(first job: Marvell Technology Group Ltd.)
Xiuyuan Bi: M.S., 2010.09-2011.12(Continue Ph.D. program in Pitt)
Yi-Chung Chen: M.S., 2010.01-2011.08(Continue Ph.D. program in Pitt)
Chao Zhang: M.S., 2009.09-2010.08(first job: LSI Corp.)
Gengyuan Zhang: M.S., 2009.09-2010.08(first job: Inphenix Inc.)
Xiao Wang: M.S., 2009.09-2010.08
Miao Hu: M.S., 2009.09-2011.08(Continue Ph.D. program in Pitt)
- *Supervised Students as Committee Member*
- Wujie Wen: Ph.D., 2011.09-2015.07(expected)
Beiye Liu: Ph.D., 2011.12-2015.12(expected)
Yu Du: Ph.D., 2014.01-2014.12(expected)
Haifeng Xu: Ph.D., 2012.04-
Bo Zhao: Ph.D., 2012.11-2013.12(first job: Apple Inc.)
Yong Li: Ph.D., 2012.11-2013.12(first job: WMware)
Yaojun Zhang: Ph.D., 2010.09-2014.12(expected)
Yirong Zhao: M.S., 2011.09-2013.08
Harika Manem: Ph.D., 2009.09-2011.12(first job: University at Albany)
Najla Alfaraj: Ph.D., 2009.09-2011.12(first job: College of Technological Studies in Kuwait)
Zhan Ma: Ph.D., 2009.09-2011.01(first job: Samsung Research)
- *Visiting Students*
- Xiaofang Hu Ph.D., City U. of HK, HK; 2013.12-2014.05
- *Visiting Professors*
- Tao Cai Associate Professor, Jiangsu University, China; 2013.10-2014.10
Dejiao Niu Associate Professor, Jiangsu University, China; 2013.10-2014.10
Meng Zhang Associate Professor, Northwestern PolyTech University, China; 2014.08-2015.08