The Stochastic Characteristics of Memristor Devices and Case Studies in Neuromorphic Hardware Design

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As traditional von Neumann computing systems based on CMOS technologies gains less performance increment and energy efficiency from device scaling, neuromorphic hardware systems that potentially provide the capabilities of biological perception and information processing within a compact and energy-efficient platform have gained great attentions [1][2]. However, the hardware development of neural networks in traditional VLSI circuits still falls behind from the following perspectives. First, the weight matrix storage by digital-analog convertors, capacitors, or floating gates, has low precision, high power consumption, and high area overhead. Second, the voltage-based matrix computation induces many design issues including voltage offset, noise generation and voltage saturation. Last but not the least, the architecture and connection of such neuromorphic systems are hard to scale up, limiting the size and function of hardware implementations [3].

Theoretically, an idea memristor exhibits similarly as a synapse in bio-tissues [4]: it "remembers" the total electric flux through the device as its memristance M, which can be leveraged as the weight between an input voltage and an output current such as $I = V / M$. Such device feature potentially provides a complementary solution in neuromorphic design.

However, at current stage, a large gap exists between the theoretical memristor characteristics and the experimental data obtained from real devices, raising severe concerns in feasibility of memristor-based hardware design. For instance, the memristor theory expresses a continuous and stable memristance change. Though an arbitrary intermediate state can be obtained by carefully setting current compliance and period in a single metal oxide memristor, the corresponding realization at large scale, e.g., crossbar array, is very difficult after including intrinsic design constrains, process variations, etc. Keeping a memristor in its ON or OFF state (R_{on} or R_{off}), on the contrary, is much more controllable. Thus, memristors nowadays are utilized as "memristive switches". Moreover, metal oxide based memristor behaves stochastically and hence even a single memristive device demonstrates large variations in performance. More specific, the static states of a single memristive switch, i.e., R_{on} and R_{off}, are not fixed, but have large variations with skewed distributions and heavy tails [5]. The switching mechanism of a memristive switch, that is, its dynamic behavior, performs as a stochastic process [6], which has been widely demonstrated in various materials. Previous statistical analyses on memristors were limited to the binary switching as data storage. It is necessary to understand and model the analog stochastic characteristic of memristors.

In this work, we built a stochastic behavior model of TiO_2 memristive devices based on the real measurement results to better facilitate the exploration of memristive switches in hardware implementation. The model bypasses material-related parameters while directly linking the device analog behavior to stochastic functions. Simulations (Figure 1 and Figure 2) show that the proposed stochastic device model fits well to the existing device measurement results.

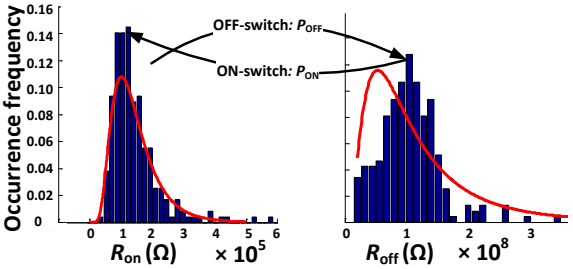

Figure 1. The static state distributions of a memristive switch.

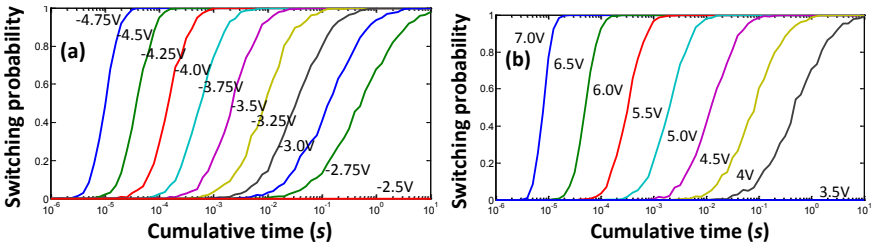

Figure 2. The time dependency of ON (a) and OFF (b) switching at different external voltages *V*.

To overcome the gap between the theoretical and real characteristics of memristive devices, we propose a macro cell design illustrated in Figure 3, which is composed of a group of parallel connected memristive switches. It utilizes multiple memristors to represent an analog value by leveraging the stochastic behavior. Though the design sacrifices the design density, it is still more efficient than the CMOS implementations in floating gates or capacitors. The usage of macro cells in weight storage unit and stochastic neuron, the two fundamental elements of neuromorphic system, is then demonstrated. The macro cells can be naturally integrated into memristor crossbars that previously were proposed as weight storage in neuromorphic computation.

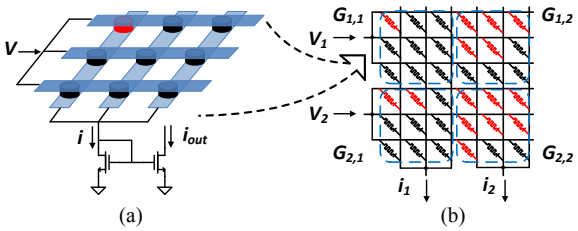

Figure 3. (a) A macro cell containing of 9 memristive switches on a 3x3 crossbar. (b) Partitioning a 6x6 memristive switch crossbar to obtain a 2x2 macro cell crossbar for continuous weight storage.

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